HOMEWORKS

Phase-Lock Basics, 2nd Edition

1.1 Refer to Fig. 1.1. For the phase detector, $\Theta=\pi$ radians. The VCO has $\varphi_{out}(t) = (\omega_c + K_v u_2)t$. The loop is locked. Fill in the remainder of the following table. Row (a) is done as an example, with the answers shown in ***italic*** script.

	K_p	φ_{in}- φ_{out}	$u_1 = u_2$ volts	ω_c or f_c	K_v	$d\varphi_{in}/dt$
(a)	0.02 V/deg	220°	***0.8***	10^3 rad/sec	100 rad/sec/V	***1080 rad/sec***
(b)	0.16 V/rad	3.14 rad		10^4 Hz	100 Hz/V	
(c)	10 V/rad		-12		2 Hz/V	180 Hz
(d)	20 V/c			100 Hz	2 Hz/V	104 Hz
(e)	2 V/c	0.75 c		2 GHz		2020 MHz
(f)	2 V/c			17 MHz	1 MHz/V	18.5 MHz

1.2 Over what range of frequency (lowest and highest possible values of $d\varphi_{in}/dt$) can the loop of row (f) in Problem 1.1 maintain lock if the phase detector has a sawtooth characteristic as in Fig. 1.4 (with $\Theta=\pi$ radians still)? Is the state described by row (f) possible?

1.3 Over what range of frequency (lowest and highest possible values of $d\varphi_{in}/dt$) can the loop of row (f) in Problem 1.1 maintain lock if the phase detector had a sinusoidal characteristic, as in Fig. 1.5? The midvoltage corresponds to f_c.

2.1 A first-order PLL has an open-loop gain of 50 at f_m = 100 Hz. Show that its open loop gain $|G(1\ Hz)|$ at 1 Hz is 5000. At what frequency is the gain one? What is the phase shift $\angle G(1\ \mathrm{Hz})$?

2.2 In Fig. 2.4, $K_p = 0.1$ V/c, $K_{LF} = 3$, $K_v = 1$ MHz/V.
(a) Show that unity open-loop gain occurs at 47.75 kHz.
(b) If K_p is changed to 1 V/rad, what is the unity-gain frequency (include units—always)?

2.3 In Fig. 2.7, $K = K_p K_{\mathrm{LF}} K_v = 1000\ \mathrm{sec}^{-1}$ and ω_{in} has a step increase of 100 rad/sec.
(a) Sketch the transient at ω_{out} and indicate its amplitude.
(b) How long will it take ω_{out} to come within 1 rad/s of its final steady-state value?
(c) Sketch the transient frequency error at ω_e, label its amplitude and show its final value.
(d) How long will it take for the frequency error to come within 10 Hz of its final steady-state value?
(e) Sketch the change in the phase error φ_e, label its amplitude, and show its final value.

3.1 In Fig. 3.2*b*, $V_{p\text{-}p} = 1.5$ V. What is K_p (include units—always)?

3.2 In Fig. 3.5(a), $I = 3$ mA.

(a) What is K_p?

(b) In Fig. 3.5*b*, $V_x = 0$ and $V = 2$ V. What is R_x to give the same K_p as in 3.5*a*?

(c) If V_x changes to 2 V, what change should be made in Fig. 3.5*b* to maintain the same PD characteristic?

3.3 In Fig. 3.19, $R_1 = 1$ kΩ, $R_2 = 100$ Ω, $C = 1\mu$F.

(a) Write *F(s)* for this filter.

(b) What are its gain and phase shift at 500 Hz?

3.4 In Fig. 3.25, $R_1 = 1$ kΩ.

(a) What are the values of R_2 and C in Fig. 3.23*c* to give a high-frequency gain of 5 and a 1-Hz gain of 100?

(b) What value would R_p have in Fig. 3.23*d* to limit the gain to 1000?

(c) What are the values of the components in Fig. 3.23*g* to give a pole at 20 Hz, a zero at 100 Hz, and a DC gain of 100?

3.5 In Fig. 3.21, $R_1 = 10$ KΩ and $C = 1000$ pF.

(a) What configuration for Z_{FB} in Fig. 3.25 will give the same response (excepting an inversion) and what will be the component values if $R_1 = 1$ kΩ in Fig. 3.25?

(b) What configuration will give the same response as in Fig. 3.21 when driven by the circuit of Fig. 3.5*a*? What will be the capacitor value if the resistor is 10 kΩ?

(c) What will be I in Fig. 3.5*a* for $K_p K_{\mathrm{LF}} = 0.2$ V/rad?

4.1 **(a)** What are the damping factor ζ and natural frequency ω_n for a loop having an open-loop gain of 1000 at $\omega = 1$ rad/sec and a lag-lead filter with $\omega_p = 10$ rad/sec and $\omega_z = 200$ rad/sec?

(b) What are ζ and ω_n for such a loop without a zero (lag filter)?

(c) What are ζ and ω_n for the loop in (a) except that it has no nonzero filter pole (integrator-and-lead filter)?

(d) What are ζ and ω_n for the loop in (a) if the same value of $K\omega_p$ is maintained while $\omega_p \to 0$?

4.2 **(a)** Write the phase transfer function $\varphi_{\text{out}}(\omega)/\varphi_{\text{in}}(\omega)$ for a closed loop with a lag-lead filter as shown in Fig. 3.19 and with the following parameters: $R_1 = 2$ kΩ; $R_2 = 200$Ω; $C = 10$ μF; $K_p = 0.5$ V/rad; $K_v = 10^4$ (rad/sec)/V.

(b) If a phase modulation of peak deviation 0.01 rad appears at the input with a modulation frequency of 50 Hz, what will be the peak deviation of the output phase at 50 Hz?

(c) What if the modulation frequency increases to 5 kHz?

(d) If the input is modulated with 10 Hz peak frequency deviation at a 50 Hz rate, what will be the output peak frequency deviation?

5.1 **(a)** Sketch a Bode gain and phase plot for a loop where $K_p = 1$ V/cycle, $K_V = 3.5$ kHz/V, and the filter is shown in Fig. 3.19 where $R_1 = 1$ kΩ, $R_2 = 100$ Ω, and $C = 1$ μF.
(b) What are the gain and phase margins?

5.2 Give gain and phase margins and the frequencies at which they occur for a PLL with $K = 10^4$ sec^{-1} and whose filter has a pole at 1 kHz, two poles at 8 kHz, and a zero at 2 kHz.

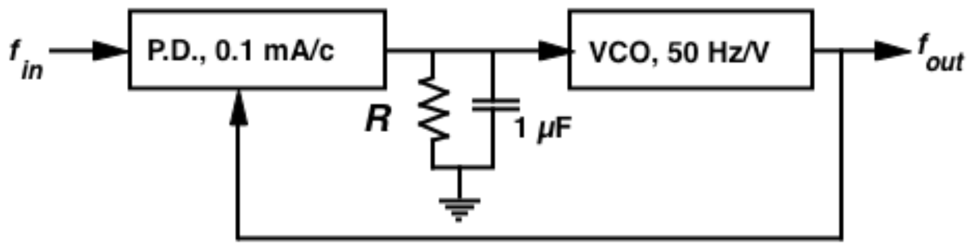
5.3 Pick the value of R_1 in the filter of Fig. 3.19, with $R_2 = 2$ kΩ and $C = 0.2$ μF, and the value of K for the loop to give 45° phase margin and a unity-gain bandwidth frequency $f_L = 200$ Hz.

5.4 What is the gain margin for a loop with a gain of 10^6 at 1 Hz and filter poles at 100 kHz and 10 MHz?

6.1 A PLL has an integrator-and-lead filter, Figs. 3.23(c) and 3.25 with $R_1 = 2$ kΩ and $G \Rightarrow \infty$. $K_p = 1$ V/rad and $K_v = 1$ MHz/V. The loop is locked and following an input frequency ramp of 100 MHz/sec. The steady voltage u_1 at the input to the loop filter is 1 V. The answers to the following questions should not involve many equations. If you think about them properly, they are simple.
(a) What is the size of C in the loop filter?
(b) What is the value of the phase error?

6.2 A PLL has the loop filter in Fig. 3.21 with $R_1 = 1$ kΩ and $C = 0.014$ μF. The VCO tuning curve is linear with 999 kHz at 3 V and 996 kHz at 2.5 V. The phase detector is a flip-flop with output states of 0.5 and 3.5 V. Give the following (including units of course):
(a) Minimum input frequency at which lock can occur
(b) Maximum input frequency at which lock can occur
(c) K_p
(d) K_{LF}
(e) K_v
(f) ω_p
(g) ω_n
(h) ζ
(i) ω_L (unity open-loop-gain frequency)
(j) Absolute difference between input and output phases, $\varphi_{\text{in}} - \varphi_{\text{out}}$, with 1 MHz steady input
(k) Time for the output to achieve 90% of its ultimate change after an input step (e.g., output and input phases).

6.3 For the locked loop shown below, pick R such that the first occurrence of zero frequency error is 47 ms after a frequency step input.



6.4 A PLL has a filter shown in Fig. 3.19 with $R_1 = 3$ kΩ, $R_2 = 1$ KΩ, and $C = 0.16$ μF. $K_p = 0.5$ V/rad and $K_v = 10{,}000$ (rad/sec)/V. What is the phase error in the locked loop 160 μs after a 0.2 radian input phase step?

6.5 For a loop with $\omega_n = 300$ rad/sec, $\alpha = 1$, $\zeta = 0.5$, $K_v = 1$ kHz/V, what is the peak phase error φ_e in response to a 1 V step added to the tuning voltage and at what time does it occur?

6.6 For a loop with $\omega_n = 1000$ rad/sec, $\alpha = 1$, $\zeta = 1$, the VCO center frequency ramps at 10 Hz/ms due to temperature changes. What is the resulting phase error φ_e?

7.1 $f = 10$ MHz + 1 kHz cos(200 rad/sec $t + \pi/4$ rad)

(a) What is the carrier frequency?
(b) What is the peak frequency deviation?
(c) What is the modulation frequency?
(d) What is the peak phase deviation?
(e) What is the earliest time $t \geq 0$ when the frequency deviation is 0?
(f) What is the earliest time $t \geq 0$ when the phase deviation is 0?

7.2 Given a first-order loop and $K_p = 0.1$ V/rad.

(a) When the reference has a peak deviation of 0.1 rad, what will be the peak deviation of the phase detector output at high modulation frequencies?
(b) What is the value of K_v for a frequency-demodulation response at $f_m = 1$ kHz that is 6 dB below the DC response.
(c) If $K_v = 1$ kHz/V, at what modulation frequency will the phase demodulation output be 20 dB below its high frequency value?
(d) What peak voltage injected after the phase detector will produce 0.01 rad peak phase deviation at low frequencies?

7.3 The reference frequency input to a second-order loop with a low-pass filter is swept in modulation frequency. The frequency deviation of the output (VCO) equals that of the input at low modulation frequencies but peaks 5 dB higher than the input deviation when a modulation frequency of 1 kHz occurs ("peaks" meaning that is the highest response).

(a) What is the damping factor?

(b) As the modulation frequency increases, at what frequency will the output deviation again equal the input deviation?

7.4 A loop is used as a phase modulator. The modulating voltage, that is added at the phase detector output, is swept in frequency with a 1-V peak sine wave. At low frequencies the peak phase deviation produced is 0.1 rad. It is a maximally flat response with -3 dB at 10 kHz.

(a) What is K_p ?

(b) What are α and ζ.

(c) What is ω_n?

7.5 A loop has an integrator-and-lead filter with unity open-loop gain (straight-line gain approximation) at 10 kHz and a zero at 5 kHz. What is the peak phase error when the input reference signal is frequency modulated at a peak deviation Δf = 4 kHz? At what frequency f_m does it occur?

7.6 A frequency modulator with a frequency range that extends well below the loop bandwidth is represented by the block diagram as in Fig. 7.18*b*. The amplifier gain is 100. K_pK_v = 1000 sec^{-1}. R = 10 kΩ.

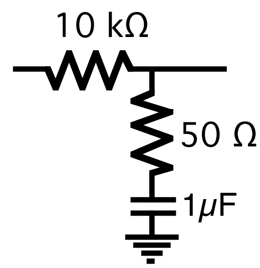
(a) What should be the value of C.

(b) The loop has an integrator-and-lead filter with ζ = 1. If the input Δu_1 were removed, by how much would the frequency deviation drop at a modulation frequency equal to half of the natural frequency?

(c) If both ω_m and the magnitude of the frequency deviation equal ω_n /2 when Δu_1 is connected, what will be the magnitude of the phase error after the input at Δu_1 is disconnected [same loop as in (b)]?

7.7 Using Figs. 7.8 to 7.11, confirm the theory of Section 7.8.5.1 by showing equal responses at $\omega_m = 0$, $\omega_m = \omega_n$, and $\omega_m = 10\omega_n$.

8.1 A loop has a balanced mixer phase detector with a (maximum) gain of $K_p' = 0.1$ V/cycle. The tuning characteristic of the oscillator has a 40-MHz/V slope. The loop filter is shown below. The VCO is 90° out of phase with an input signal to which it is locked when the frequency is 30 MHz.



(a) If the input frequency drifts, how high can it go before the loop will lose lock? Give frequencies in both radians/second and hertz.

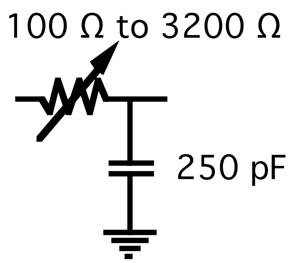
(b) After lock is broken, the input frequency is lowered again. At what frequency can lock be reacquired? What are the restrictions on the formula that you used and how well are they met (give numerical values)?

(c) At what difference between input frequency and VCO center frequency ω_c will cycle skipping stop? What are the restrictions on the formula that you used and how well are they met (give numerical values)?

(d) How long will it take to stop cycle skipping if the input signal is 14 kHz above f_c? What are the restrictions on the formula that you used and how well are they met (give numerical values)? Compare the answer you get from a formula to the value given by Fig. 8.18.

(e) Repeat (d) for an initial 6 kHz mistuning.

8.2 The filter in the loop described above is changed to that shown below but the phase-detector and VCO gain constants remain the same.



(a) What is the total range over which the input frequency can be acquired (difference between minimum and maximum frequencies) when the variable resistor is set at its highest value?
(b) What is the total range when the resistor goes to minimum value?

8.3 A loop false locks 100 kHz above the input frequency. At that offset, a narrow IF filter has caused 120° of effective phase lag and a 3-dB gain drop in the loop. The loop has an lag-lead filter with the pole at 2 kHz and the zero at 20 kHz. What is K under the following conditions:
(a) The VCO center frequency f_c equals the input frequency f_{in}?
(b) The VCO center frequency f_c is 50 kHz higher than the input frequency f_{in}?

8.4 A loop must have 100 kHz bandwidth. It has a lag-lead filter with a 10 kHz zero frequency. Pull-in range is to be ±500 kHz.
(a) What is the largest uncompensated phase-detector offset that can be tolerated?
(b) What should the filter pole frequency be?

9.1 A loop has $\zeta = 0.7$, $\omega_n = 500$ rad/sec, and $K'_p = 0.2$ V/rad. The loop filter is integrator and lead.

(a) How fast can the VCO's center frequency be swept past the reference frequency with certainty that the loop will lock?

(b) What steady-state phase error will it acquire after lock at this sweep speed?

(c) If the same phase detector is used as a coherent detector (assuming they act as ideal multipliers), how high can the threshold at its output be set to insure that lock will be detected at this maximum sweep rate?

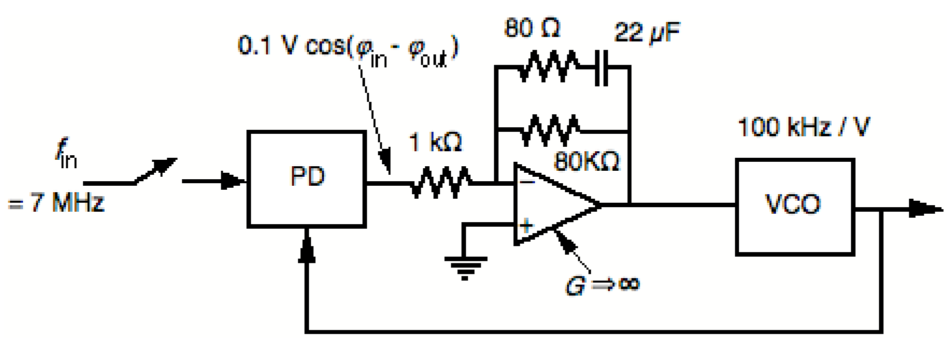
(d) After the sweep input is removed, the loop remaining in lock, what will become the steady-state output from the coherent detector?

9.2 A loop has $\omega_n = 500$ rad/sec and $K'_p = 0.2$ V/rad. The loop filter is lag-lead. The reference frequency is swept past the VCO center frequency at 1 kHz/sec. After the loop locks to the sweeping signal, the phase detector output ramps at a rate of 1.8V/sec. What is K?

9.3 The reference input is sweeping at 10 kHz/sec when it is connected to the loop. The loop is a "high-gain loop" with a natural frequency of 140 Hz and a filter zero at 100 Hz. How far can the reference have swept past the VCO center frequency when the connection is made if lock is to be certain?

9.4 What is the maximum open-loop sweep rate for 99% probability of detection if the decision filter has a bandwidth of 1 kHz and the threshold is set at 60% of the maximum output from the coherent detector?

9.5 Refer to the figure below.



(a) After the switch is closed, over what range of center frequencies f_c (which occurs when the phase detector output is zero) will the loop lock without skipping cycles?

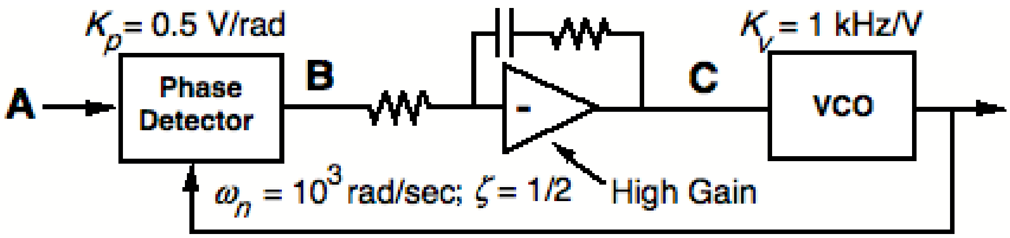
(b) Over what range of f_c will the loop eventually lock?

(c) If the center frequency is 7.00500 MHz, how long will acquisition take?

(d) Once lock is achieved, how high can the VCO center frequency drift without loss of lock?

(e) What is the shortest time required to sweep (closed loop) the VCO center frequency by 2% (from 0.99 f_{in} to 1.01 f_{in}) to insure acquisition in the absence of noise?

11.1 Complete the following table for the loop below. Note that the two conditions specified "At **A**" for a given ω_m (e.g., lines one and two) do not necessarily occur simultaneously.



ω_m	At **A**	At **B**	At **C**
10 rad/sec	$\varphi_{rms} = 10^{-2}$ rad	______V rms	______ V rms
"	$S_\varphi = 10^{-4}$ rad^2/Hz	______ V^2/Hz	______ V^2/Hz
2500 rad/sec	$\varphi_{rms} = 0.01$ rad	______V rms	______ V rms
"	$S_\varphi = 0.001$ rad^2/Hz	______ V^2/Hz	______ V^2/Hz
700 rad/sec	$S_\varphi = 2\times10^{-5}$ rad^2/Hz	______ V^2/Hz	______ V^2/Hz

11.2 What is the mean square phase in the region between 1 kHz and 3 kHz if the phase power spectral density at 1 kHz is $S_\varphi = 10^{-4}$ rad^2/Hz and it slopes down at -9 dB/octave?

11.3 **(a)** Derive

$$\int_{f_1}^{f_2} S_\varphi df = \frac{f_1 S_\varphi(f_1)}{b+1}\left[\left(\frac{f_2}{f_1}\right)^{b+1} - 1\right].$$

(b) Show by algebraic manipulation of the right side above that

$$\int_{f_1}^{f_2} S_\varphi df = \frac{f_2 S_\varphi(f_2)}{b+1}\left[1 - \left(\frac{f_1}{f_2}\right)^{b+1}\right].$$

11.4 The VCO output from a PLL is modulated by flat phase noise extending from 0 to 10 kHz.

(a) What is the phase power spectral density S_φ, in rad^2/Hz, that causes a 3 dB reduction in the power of the main signal (carrier)?

(b) How great would be the reduction, in dB, if S_φ were cut in half?

12.1 Figure P12.1 below shows the phase power spectral density at the input of the loop of Fig. 12.13. Sketch the phase power spectral density at A and at B on this figure or a similar chart. Use straight-line approximations; indicate slopes and levels.

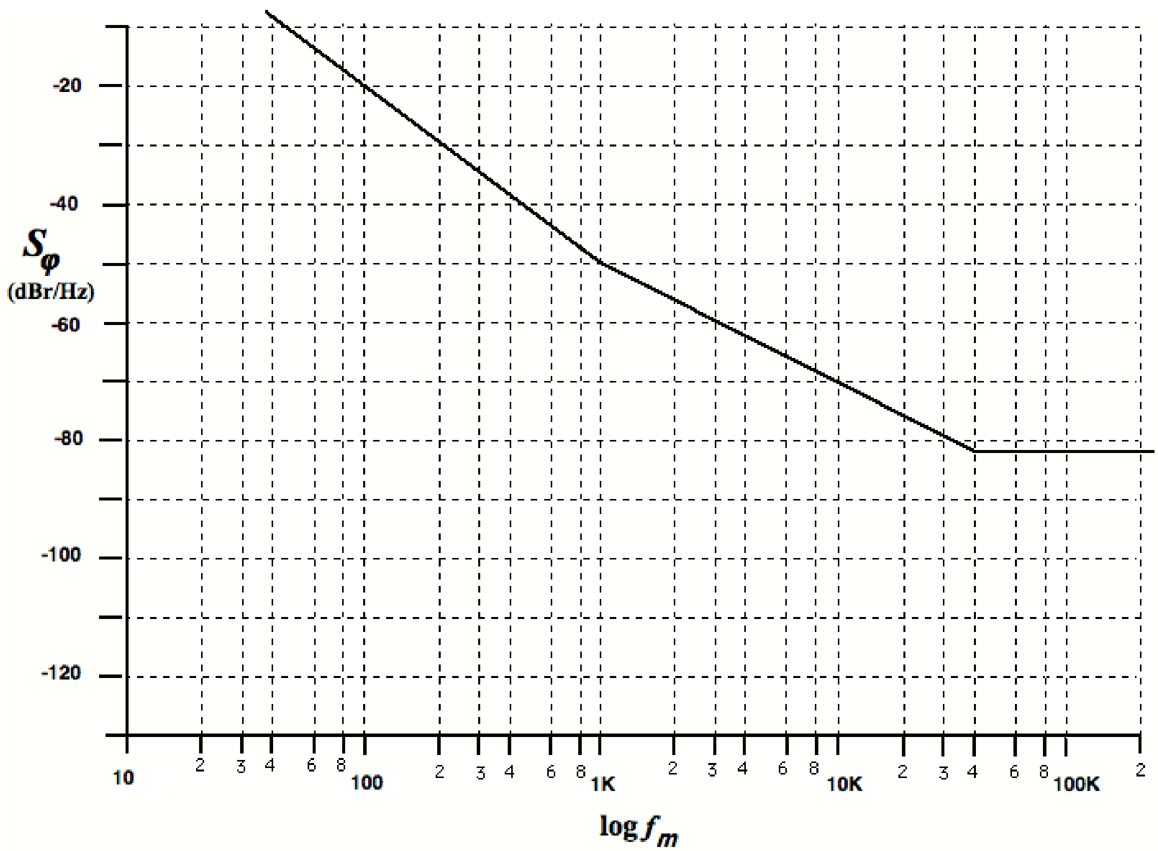


Fig. P12.1

12.2 What is the variance of phase, $\sigma_\varphi{}^2$, between 100 Hz and 200 kHz indicated by the density S_φ shown in Fig. P12.1? Show separately the calculations for each of the regions defined by different slopes. Give answers in units of radians squared for (a) 100 Hz to 1 kHz, (b) 1 kHz to 40 kHz, (c) 40 kHz to 200 kHz, and (d) the total variance for the three regions combined.

12.3 What equivalent input noise voltage density for the op amp in Fig. 12.13 will produce $S_f = 10^{-6}$ Hz, at 1 kHz modulation frequency, at the loop output? (The equivalent noise voltage is in series with the positive (non-inverting) input of the op amp. The transfer function from the positive input to the op-amp output is $1 - G_A$, where G_A is the transfer function from the PD output to the op amp output. Note that, when G_A is real, as when the capacitor impedance goes to zero, it is negative.)

12.4 If the PPSD shown in Fig. P12.1 is due to the VCO and the reference PPSD level is –70 dBr/Hz, what is the approximate unity-gain bandwidth to minimize phase variance at the loop output?

12.5 In Fig. 12.17 the PLO has negligible residual noise. It is a type-2 loop with $f_n = 1$ kHz and $\zeta = 1$. The measured PD sensitivity is $K_p = 0.1$ V/cycle. A spectrum analyzer connected to the PD shows -90 dBm at 800 Hz in a 50 Ω measurement system. The noise bandwidth is 3 Hz. What is $S_\varphi(800\text{ Hz})$ from the DUT?

13.1 A one-sided random-noise power spectrum is shown below at (a) along with a signal that serves as a "carrier" for the noise. Give the values *A* through *D* for the various representations of the noise.

L is the single-sideband relative power spectral density (one sided).
L_φ is that part of L that is due to phase noise.
$S_{1\varphi}$ and $S_{2\varphi}$ are the one-sided and two-sided phase power spectral densities respectively.
"dBm/Hz" means dB relative to 1 mW per Hz.
"dBc/Hz" means dB relative to the carrier power per Hz.
"dBr/Hz" means dB relative to 1 radian^2 per Hz.

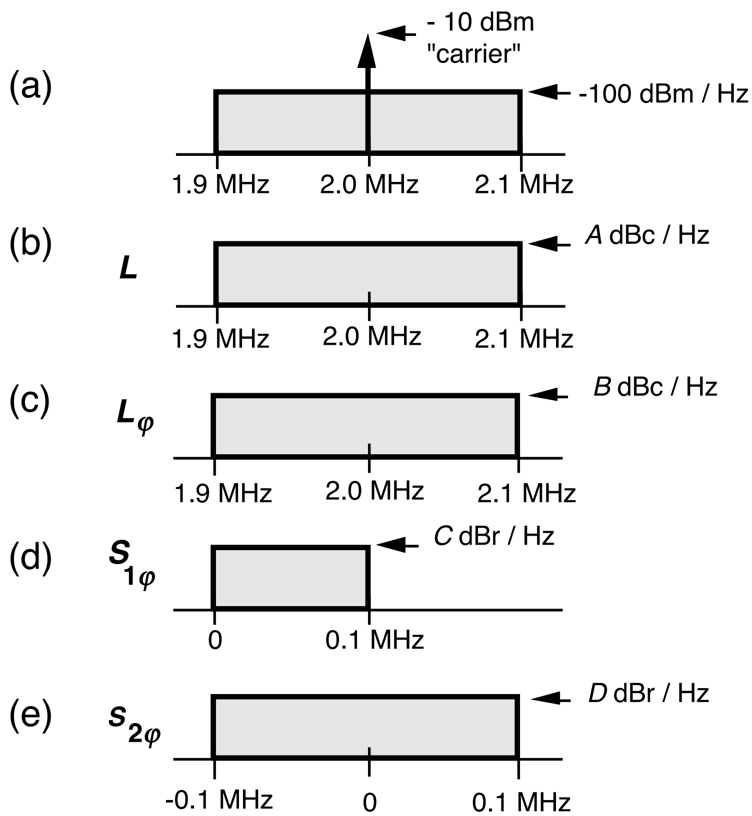


Fig. P13.1

13.2 The noise shown below accompanies the 10 mW carrier into the loop shown. The loop has $\omega_n = 2\square\times2\times10^5$ rad/sec and $\zeta = 1$.

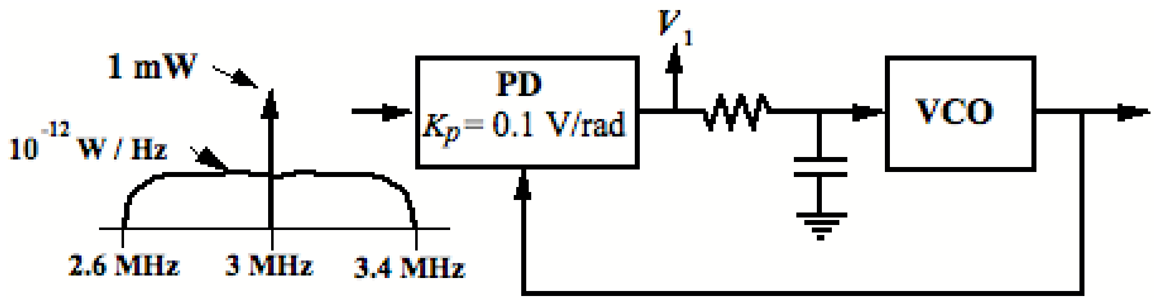


Fig. P13.2

(a) Sketch the power spectrum at V_1. Show width, shape, and magnitude.
(b) Sketch the phase power spectral density S_φ at the VCO output. Show width, shape, and magnitude.
(c) Sketch the sideband density (as one might see on a spectrum analyzer) at the VCO output. Show width, shape, and magnitude.

HINT: see Example 14.1.

13.3 A triangular PD characteristic can be represented by a series of sinusoids that are the components of its Fourier series. With the linear range between $-\pi/2$ and $+\pi/2$, the spectrum consists of odd harmonics. With K'_p = 1V/rad, the nth harmonic is $\frac{4\text{ V}}{\pi n^2}\sin(n\varphi_e)$.

(a) Show that (in the absence of noise) the first 5 terms give the correct peak amplitude to within 5%.

(b) Find the amplitude in the presence of Gaussian phase noise with an rms value of 1 rad, using the first five terms. [The accuracy will be better than 0.01% in this case. Why is it so much better than in part (a)?]

(c) What is the amplitude of the sinusoidal characteristic for the conditions of parts (a) and (b)?

14.1 Give the one-sided noise bandwidth B_n in Hz for the following.

LOOP FILTER TYPE	ω_n (rad/sec)	ζ	K(sec^{-1})
(a) Low Pass	1000	0.5	
(b) Integrator and Lead	10^4	0.2	
(c) None			10^4
(d) Lag-Lead	100	0.5	200

14.2 Find the one-sided noise bandwidth for the loop shown below. Give units.

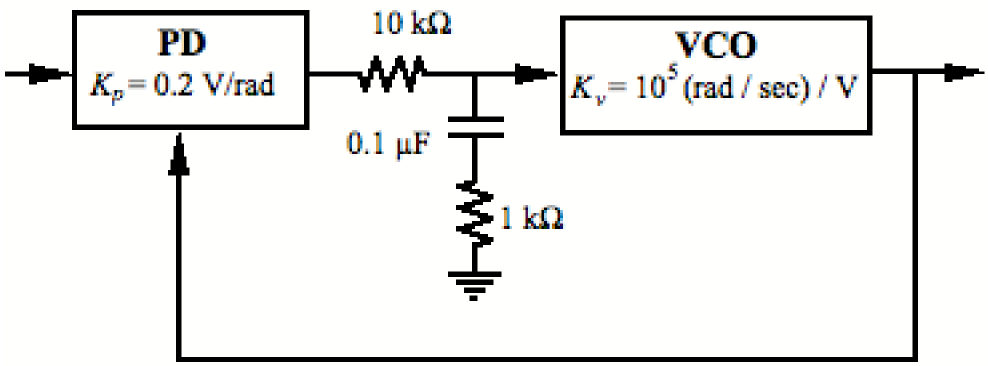


Fig. P14.2

14.3 A loop is to follow a 1-MHz input frequency step while limiting the integrated square difference between input and output phase to a maximum of

$$E^2 = \int_0^\infty [\varphi_{\text{out}} - \varphi_{\text{in}}]^2 \, dt = 0.01 \, \text{rad}^2 - \text{sec}$$

and minimizing the mean square output phase noise, $\sigma^2_{\varphi,\text{out}}$.

(a) What kind of loop (order, filter type, damping factor) should be used?

(b) The input signal power is 1 mW and the noise density is 1 mW spread evenly (flat) over 1 MHz. What should be ω_n and what will be the value of $\sigma_{\varphi,out}{}^2$?

15.1 The loop shown below is driven by a frequency-modulated signal, which is embedded in noise as indicated by the power spectrum shown. (Hint: section 7.8.1 should be useful here.)

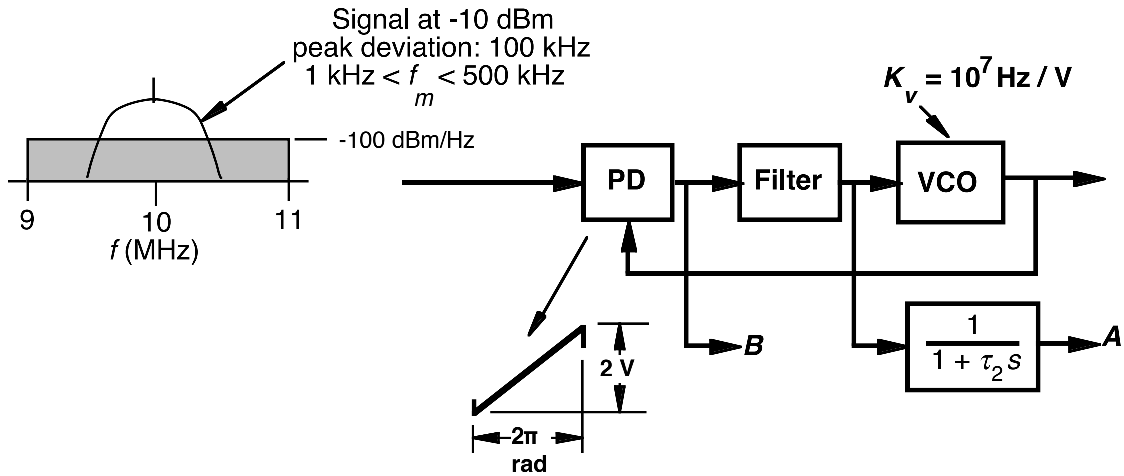


Fig. P15.1

(a) What is the peak signal output at A if the response is flat with modulation frequency?
(b) What is ω_n to give -3 dB response to FM at the maximum modulation frequency? Use a high-gain [$F(s) \approx (1+\tau_2 s)/s$] loop with $\zeta = 1/\sqrt{2}$ to frequency demodulate the signal, taking the output at *A*.
(c) Why use $\zeta = 1/\sqrt{2}$?
(d) How much noise power appears at *A* (assume 1Ω)?
(e) What is the maximum peak phase error deviation at any single frequency (due to signal modulation) ?
(f) At what modulation frequency does that occur?
(g) Approximately how much noise appears at *B* (assume 1 Ω)?
(h) What is the lowest modulation frequency for which accurate phase demodulation could be obtained at *B* (the -3 dB frequency)? (This is not related to the FM input spectrum shown above.) What is the -1 dB frequency?

16 Assume one-sided noise and bandwidths and additive white noise, unless otherwise indicated, in the following (Chapter 16) problems.

16.1 Compare phase margins exactly in this problem. Do not use straight-line approximations for gain or phase. The objective is to discover the effects of noise on parameters, including phase margin, and we should not allow it to be masked by approximations. The block diagram in Fig. P16.1 shows parameters representative of the loop when it is tested with a strong input signal ($\rho >> 1$).

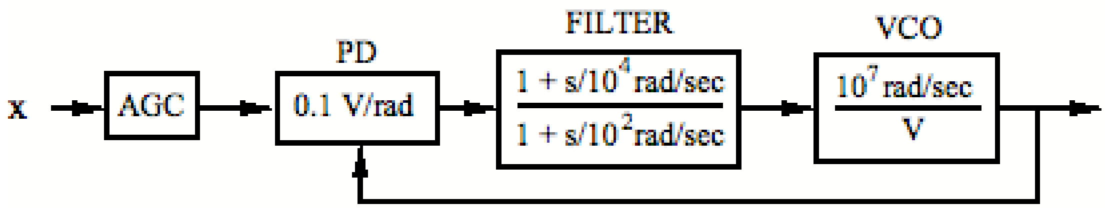


Fig. P16.1

(a) What is the phase margin in degrees?

(b) What is the noise bandwidth in hertz?

When the loop is used with a signal that is accompanied by noise of twice the power level of the signal, an AGC circuit maintains the same total power level at its output as during test. Under these circumstances:

(c) What is the phase margin in degrees?

(d) What is the noise bandwidth in hertz?

(e) If the signal and noise powers at **x** are equal, approximately by how much will the phase margin and noise bandwidth change if the AGC is replaced by a limiter (K_{p0} fixed)?

(f) With twice as much noise power as signal power into the AGC, what will be the signal to noise ratio at its output in decibels?

(g) Under these same conditions at the input to a limiter, what will be the signal to noise ratio at its output in decibels?

16.2 A limiter operates with an input noise level 3 dB below the input signal.
(a) If the noise is additive Gaussian noise, what will be the output signal-to-noise ratio of the limiter in decibels?
(b) If the noise is phase noise, what will be the output signal-to-noise ratio in decibels?
(c) If it is amplitude noise, what will be the output signal-to-noise ratio in decibels?

16.3 A circuit similar to Fig. P16.1 is driven by a signal and additive noise. The *S/N* at the AGC output measures 17 dB while the phase variance at the loop output is (20 mrad)^2. Another identical circuit is similarly driven through a limiter and the *S/N* also measures 17 dB at the loop input (limiter output). What is the variance of phase from that loop?

17.1 Repeat Example 17.1 except use a signal strength of -6 dBm.

17.2 Given: First-order loop;
Signal power 1 mW;
One-sided additive noise density 10^{-8} W/Hz;
Loop one-sided noise bandwidth 50 kHz.
Find the mean frequency of cycle skipping ($\bar{F}$).

17.3 Given: additive input noise producing 0.25 rad^2/Hz equivalent S_ϕ (1-sided);
integrator-and-lead filter; $\zeta_0 = 0.707$;
initial phase and frequency errors are zero.
(a) Find ω_{n0} to give a mean time until the first cycle skip of 1 sec. Hint: This can be done by plotting the desired value on the same graph that shows the actual value.
(b) What is the expected cycle skip rate under these conditions for a high-gain ($\alpha \approx$ 1) loop? Explain your estimate and specify any required parameters.
(c) What is the probability that a cycle will be skipped in the first 0.6 sec?
(d) What is the actual output phase variance when the 1-sided noise bandwidth is reduced to 2 Hz?

18.1 A second-order loop is locked to a signal in the presence of additive noise. The true variance of the output phase is 0.5 rad^2.

(a) What would be the variance if the loop were linear and had an integrator-and-lead filter with $\zeta = 0.707$? Compare this to the quasi-linear approximation. Repeat for a true output phase variance of 2 rad^2.

(b) What would be the variance if it were linear and had a low-pass filter? Obtain answers under the same four conditions that were used in (a).

(c) Again with the low-pass filter, suppose that, at a certain frequency, the phase deviates from quadrature by 0.1 rad due to finite gain with no noise? What would be the mean deviation due to the noise according to the quasi-linear approximation? What value would you expect in fact? What would these values be if the output phase variance increased to 2 rad^2?

18.2 A loop has an integrator-and-lead filter. The filter zero is at 150 Hz and the open-loop gain is unity at 50 Hz.

(a) What is the phase margin in degrees?

(b) A binary phase modulation of ±60° at a 20-kHz rate is added to the input. What is the phase margin then?

18.3 A high-gain ($K >> \omega_n$) second-order loop has a lag-lead filter, a natural frequency ω_n of 500 rad/sec, and a damping factor ζ of 0.5. The input signal power is -10 dBm and the noise power in a band from 0 to 500 kHz is -13 dBm. The input carrier frequency equals the VCO center frequency, 250 kHz. Give answers in units of radians squared.

(a) What is the phase variance $\sigma_{\varphi n}{}^2$ at the loop output?

(b) What is $\sigma_{\varphi n}{}^2$ if the input signal is phase modulated ±45° with equal probability of either state? Here, and below, assume the frequencies of the modulation are well beyond the loop bandwidth.

(c) What is $\sigma_{\varphi n}{}^2$ if the signal is phase modulated with information that has a noise-like Gaussian distribution with $\sigma = 0.7$ rad?

(d) What is $\sigma_{\varphi n}{}^2$ if the input is phase modulated with a sinusoid of peak deviation 45° [$J_0(\square/4) = .85$].

18.4 What values of the following parameters will reduce the effective loop gain by 1.9 dB ($\eta = 0.8$)?

(a) S_i/N_i in a limiter [$B_n << W$] in decibels

(b) S/N, $\rho_{L0} = 1/\sigma_{\varphi 0}^2$, in the loop [$B_n << W$; integrators & lead with $\zeta \approx 1$]

(c) $J_0(m)$ for sinusoidal phase modulation

(d) θ in rad with equiprobable binary phase modulation at $\pm\theta$

(e) $\sigma_{\varphi,\text{in}}^2$ in radians squared for Gaussian phase modulation

18.5 A loop has $K = 125{,}000\ \mathrm{sec}^{-1}$, $\omega_p = 800$ rad/sec, $\omega_z = 2550$ rad/sec.

(a) What are ω_n, ζ, α, and the noise bandwidth in the absence of additive noise?

(b) According to the quasi-linear approximation, what are these values if additive noise produces an output variance of $\sigma_{\varphi n}^2 = 0.5\mathrm{rad}^2$?

(c) What is the corresponding value of $\sigma_{\varphi 0}^2$.

(d) Estimate $\sigma_{\varphi 0}^2$ from simulation results that are shown in the text. Is the relationship between your two estimates consistent with what has been observed under other conditions?

19.1 A loop has $\alpha \approx 1$, $\zeta = 1$, and $\sigma_{\varphi 0}{}^2 = 0.2\ \mathrm{rad}^2$ due to additive Gaussian noise.

(a) What is the maximum value of $\dot{\omega}/\omega_n^2$ for 90% probability of natural acquisition, without the aid of a lock detector?

(b) If our only concern is a obtaining 90% probability of lock with a faster sweep rate, should we increase or decrease ω_n? Why?

What is the value for 99% probability of acquisition when a coherent detector is used to stop sweep and the false alarm probability is

(c) 10%, **(d)** 1%, and **(e)** 0.01%?

(f) What should be V_T / K_{pd}', the threshold setting relative to maximum possible output, when $\dot{\omega}/\omega_n^2 = 0.5$?

(g) What is the signal-to-noise ratio in the decision filter for 0.001 probability of false stop? A table of probability functions shows that SCND(3.09) = 0.999. Assume (f).

(h) What value of $\sigma_{\varphi n}{}^2$ would cause 0.001 probability of the sweep restarting due to noise. Assume the same signal-to-noise ratio in the decision filter as was used in part (g). (I.e., $\sigma_{\varphi n}{}^2$ changes due to a change in the loop, not in the coherent detector circuitry.)

20.1. The *S/N* in a rectangular filter of width 10 kHz is 3? Note: $\mathrm{erfc}\left(\sqrt{3}\right) \approx 0.0143$

(a) What is the rate of clicks in a standard discriminator following the filter?

(b) What is the rate of clicks in a discriminator using a first-order loop with a 3-dB closed-loop bandwidth (without noise) equal to the RF bandwidth of the prefilter?

(c) Estimate the rate of clicks if a limiter is inserted between the filter and the loop (with the loop's linear bandwidth preserved).

20.2 A first-order loop follows a sharp RF filter. The RF filter bandwidth is 20 times greater than the loop's noise bandwidth (video). The *S/N* in the net video bandwidth (approximately the loop bandwidth) is 3.

(a) What is the variance of the phase at the loop output?

(b) If an AGC is inserted between the filter and the loop such that the loop gain in the absence of noise remains unchanged, what will be he loop's output phase variance?

(c) If a limiter replaces the AGC, with similar maintenance of loop bandwidth, what will be the improvement (or degradation) in the output phase variance?

20.3 The S/N at the output of a first order loop is 0.5. The loop is then preceded by a first-order RF filter that maintains the same equivalent video bandwidth (i.e., half the RF bandwidth) as the loop. The bandwidths of both the filter and the loop are then widened until the original noise bandwidth is attained again. How much improvement (in dB) in output S/N will occur relative to the value without the prefilter?

20.4 Change only the value of α in the last loop used in Example 20.1, changing it from 0 to 1 and maintaining the same loop noise bandwidth. If the skip rate then increases to $\bar{F}/W = 0.0014$, what is the dynamic range.