CHAPTER X

INTEGRATED-CIRCUIT OPERATIONAL AMPLIFIERS

10.1 INTRODUCTION

The trend toward the use of operational amplifiers as general-purpose analog building blocks began when modular, solid-state discrete-component designs became available to replace the older, more expensive vacuum-tube circuits that had been used primarily in analog computers. As cost decreased and performance improved, it became advantageous to replace specialized circuits with these modular operational amplifiers.

This trend was greatly accelerated in the mid 1960s as low-cost monolithic integrated-circuit operational amplifiers became available. While the very early monolithic designs had sadly deficient specifications compared with discrete-component circuits of the era, present circuits approach the performance of the best discrete designs in many areas and surpass it in a few. Performance improvements are announced with amazing regularity, and there seem to be few limitations that cannot be overcome by appropriately improving the circuit designs and processing techniques that are used. No new fundamental breakthrough is necessary to provide performance comparable to that of the best discrete designs. It seems clear that the days of the discrete-component operational amplifier, except for special-purpose units where economics cannot justify an integrated-circuit design, are numbered.

In spite of the clear size, reliability, and in some respects performance advantages of the integrated circuit, its ultimate impact is and always will be economic. If a function can be realized with a mass-produced integrated circuit, such a realization will be the cheapest one available. The relative cost advantage of monolithic integrated circuits can be illustrated with the aid of the discrete-component operational amplifier used as a design example in the previous chapter. The overall specifications for the circuit are probably slightly superior to those of presently available general-purpose integrated-circuit amplifiers, since it has better bandwidth, d-c gain, and open-loop output resistance than many integrated designs. Unfortunately, economic reality dictates that a company producing the circuit would

probably have to sell it for more than $20 in order to survive. General-purpose integrated-circuit operational amplifiers are presently available for approximately $0.50 in quantity, and will probably become cheaper in the future. Most system designers would find a way to circumvent any performance deficiencies of the integrated circuits in order to take advantage of their dramatically lower cost.

The tendency toward replacing even relatively simple discrete-component analog circuits with integrated operational amplifiers will certainly increase as we design the ever more complex electronic systems of the future that are made economically feasible by integrated circuits. The challenge to the designer becomes that of getting maximum performance from these amplifiers by devising clever configurations and ways to tailor behavior from the available terminals. The basic philosophy is in fundamental agreement with many areas of design engineering where the objective is to get the maximum performance from available components.

Prior to a discussion of integrated-circuit fabrication and designs, it is worth emphasizing that when compromises in the fabrication of integrated circuits are exercised, they are frequently slanted toward improving the economic advantages of the resultant circuits. The technology exists to design monolithic operational amplifiers with performance comparable to or better than that of the best discrete designs. These superior designs will become available as manufacturers find the ways to produce them economically. Thus the answer to many of the "why don't they" questions that may be raised while reading the following material is "at present it is cheaper not to."

10.2 FABRICATION

The process used to make monolithic integrated circuits dictates the type and performance of components that can be realized. Since the probabilities of success of each step of the fabrication process multiply to yield the probability of successfully completing a circuit, manufacturers are understandably reluctant to introduce additional operations that must reduce yields and thereby increase the cost of the final circuit. Some manufacturers do use processes that are more involved than the one described here and thus increase the variety and quality of the components they can form, but unfortunately the circuits made by these more complex processes can usually be easily recognized by their higher costs.

The most common process used to manufacture both linear and digital integrated circuits is the six-mask planar-epitaxial process. This technology evolved from that used to make planar transistors. Each masking operation itself involves a number of steps, the more important of which are as

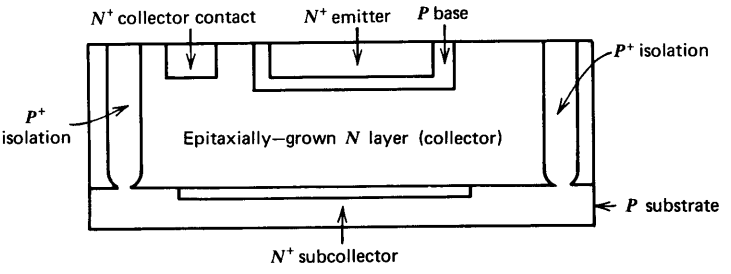


Figure 10.1 NPN transistor made by the six-mask epitaxial process.

follows. A silicon-dioxide layer is first formed by exposing the silicon integrated-circuit material to steam or oxygen at elevated temperatures. This layer is photosensitized, and regions are defined by photographically exposing the wafer using a specific pattern, developing the resultant image, and removing unhardened photosensitive material to expose the oxide layer. This layer is then etched away in the unprotected regions. The oxide layer itself thus forms a mask which permits *N*- or *P*-type dopants to be diffused into the silicon wafer. Following diffusion, the oxide is reformed and the masking process repeated to define new areas.

While the operation described above seems complex, particularly when we consider that it is repeated six times, a large number of complete circuits can be fabricated simultaneously. The circuits can be tested individually so localized defects can be eliminated. The net result is that a large number of functioning circuits are obtained from each successfully processed silicon wafer at a low average cost per circuit.

10.2.1 NPN Transistors

The six-mask process is tailored for making NPN transistors, and transistors with characteristics similar to those of virtually all discrete types can be formed by the process. The other components necessary to complete the circuit must be made during the same operations that form the NPN transistors.

A cross-sectional view of an NPN transistor made by the six-mask planar-epitaxial process is shown in Fig. 10.1.[1] Fabrication starts with a *P*-type

[1] It is cautioned that in this and following figures, relative dimensions have been grossly distorted in order to present clearly essential features. In particular, vertical dimensions in the epitaxial layer have been expanded relative to other dimensions. The minimum horizontal dimension is constrained to the order of 0.001 inch by uncertainties associated with the photographic definition of adjacent regions. Conversely, vertical dimensions in the epitaxial layer are defined by diffusion depths and are typically a factor of 10 to 100 times smaller.

substrate (relatively much thicker than that shown in the figure) that provides mechanical rigidity to the entire structure. The first masking operation is used to define heavily doped N-type (designated as N^+) regions in the substrate. The reason for these subcollector or buried-layer regions will be described subsequently. A relatively lightly doped N layer that will be the collector of the complete transistor is then formed on top of the substrate by a process of epitaxial growth.

The next masking operation performed on the epitaxial layer creates heavily doped P-type (or P^+) regions that extend completely through the epitaxial layer to the substrate. These isolation regions in conjunction with the substrate separate the epitaxial layer into a number of N regions each surrounded by P material. The substrate (and thus the isolation regions) will be connected to the most negative voltage applied to the circuit. Since the N regions adjacent to the isolation and substrate cannot be negatively biased with respect to these regions, the various N regions are electrically isolated from each other by reverse-biased P-N junctions. Subsequent steps in the process will convert each isolated area into a separate component.

The P-type base region is formed during the next masking operation. The transistor is completed by diffusing an N^+ emitter into the base. A collector contact, the need for which is described below, is formed in the collector region during the emitter diffusion. The oxide layer is regrown for the last time, and windows that will allow contact to the various regions are etched into this oxide. The entire wafer is then exposed to vaporized aluminum, which forms a thin aluminum layer over the surface. The final masking operation separates this aluminum layer into the conductor pattern that interconnects the various components.

The six masking operations described above can be summarized as follows:

1. Subcollector or buried layer
2. Isolation
3. Base
4. Emitter
5. Contact window
6. Conductor pattern

The buried layer and the heavily doped collector-contact regions are included for the following reasons. Recall that in order to reduce reverse injection from the base of a transistor into its emitter which lowers current gain, it is necessary to have the relative doping level of the emitter significantly greater than that of the base. It is also necessary to dope the collector lightly with respect to the base so that the collector space-charge layer extends dominantly into the collector region in order to prevent low collector-

to-base breakdown voltage. As a result of these cascaded inequalities, the collector region is quite lightly doped and thus has high resistivity. If collector current had to flow laterally through this high-resistivity material, a transistor would have a large resistor in series with its collector. The low-resistivity subcollector acts as a shorting bar that connects the active collector region immediately under the base to the collector contact. The length of the collector current path through the high resistivity region is shortened significantly by the subcollector. (Remember that the vertical dimensions in the epitaxial region are actually much shorter than horizontal dimensions.)

The heavily doped N^+ collector contact is necessary to prevent the collector material from being converted to P type by the aluminum that is a P-type dopant. It is interesting to note that the Schottky-diode junction that can form when aluminum is deposited on lightly doped N material is used as a clamp diode in certain digital integrated circuits.

As mentioned earlier, excellent NPN transistors can be made by this process, and the performance of certain designs can be better than that of their discrete-component counterparts. For example, the collector-to-base capacitance of modern high-speed transistors can be dominated by lead rather than space-charge-layer capacitance. The small geometries possible with integrated circuits reduce interconnection capacitance. Furthermore, NPN transistors are extremely economical to fabricate by this method, with the incremental increase in selling price attributable to adding one transistor to a circuit being a fraction of a cent.

Since all transistors on a particular wafer are formed simultaneously, all must have similar characteristics (to within the uniformity of the processing) on a per-unit-area basis. This uniformity is in fact often exploited for the fabrication of matched transistors. A degree of design freedom is retained through adjustment of the relative active areas of various transistors in a circuit, since the collector current of a transistor at fixed base-to-emitter voltage is proportional to its area. This relationship is frequently used to control the collector-current ratios of several transistors (see Section 10.3). Alternatively, the area of a transistor may be selected to optimize current gain at its anticipated quiescent current level. Thus transistors used in the output stage of an operational amplifier are frequently larger than those used in its input stage.

A recent innovation[2] used in some high-performance designs incorporates two emitter diffusions to significantly increase the current gain of certain transistors in the circuit. The oxide layer is first etched away in the emitter

[2] R. J. Widlar, "Super Gain Transistors for IC's," National Semiconductor Corporation, Technical Paper TP-11, March, 1969.

region of selected transistors, and the first emitter diffusion is completed. Then, without any oxide regrowth, the emitter regions of the remaining transistors are exposed and the second emitter diffusion is completed. The transistors that have received both emitter diffusions are sometimes called "super-β" transistors since the narrow base width that results from the two diffusions can yield current gains between 10^3 and 10^4. The narrow base region also lowers collector-to-base breakdown voltage to several volts, and precautions must be taken in circuits that use these devices to insure that the breakdown voltage is not exceeded. A second problem is that an overzealous diffusion schedule can easily reduce the base width to zero, and the price of amplifiers using super-β transistors usually reflects this possibility.

10.2.2 PNP Transistors

The six-mask epitaxial process normally used for monolithic integrated circuits is optimized for the fabrication of NPN transistors, and any other circuit components are compromised in that they must be made compatible with the NPN fabrication. One of the limitations of the process is that high-quality PNP transistors cannot be made by it. This limitation is particularly severe in view of the topological advantages associated with the use of complementary transistors. For example, the voltage level shifting required to make input and output voltage ranges overlap in an operational amplifier is most easily accomplished by using one polarity device for the input stage combined with the complementary type in the second stage. Similarly, designs for output stages that do not require high quiescent current are cumbersome unless complementary devices are used.

One type PNP transistor that can be made by the six-mask process is called a lateral PNP. This device is made using the NPN base diffusion for both the emitter and collector regions. The N-type epitaxial layer is used as the base region. Figure 10.2 shows a cross-sectional view of one possible geometry.[3] Current flows laterally from emitter to collector in this structure, in contrast to the vertical flow that results in a conventional design.

There are a number of problems associated with the lateral PNP transistor. The relative doping levels of its emitter, base, and collector regions are far from optimum. More important, however, is the fact that the base width for the structure is controlled by a masking operation rather than a diffusion depth, and is one to two orders of magnitude greater than that of a conventional transistor. There is also parasitic current gain to the substrate that acts as a second collector for the transistor. These effects originally

[3] Practical geometries usually surround the emitter stripe with a collector region. This refinement does not alter the basic operation of the device.

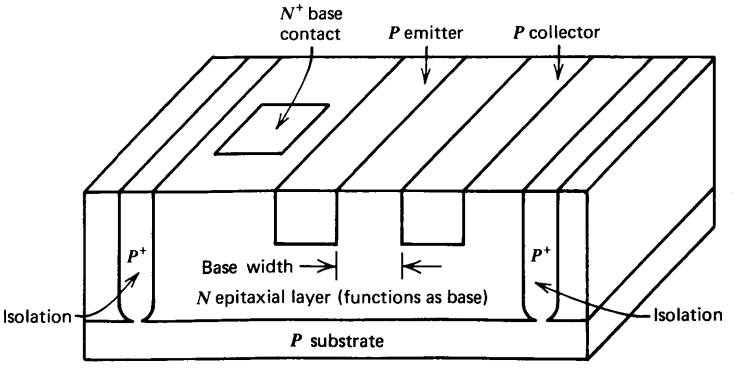


Figure 10.2 Lateral-PNP transistor.

combined to produce very low current gain, with values for β of less than unity common in early lateral PNP's. More recently, process refinements primarily involving the use of the buried layer to reduce parasitic current gain have resulted in current gains in excess of 100.

A more fundamental limitation is that the extremely wide base leads to excessive charge storage in this region and consequently very low values for f_T. The phase shift associated with this configuration normally limits to 1 to 2 MHz the closed-loop bandwidth of an operational amplifier that includes a lateral PNP in the gain path.

One interesting variation of the lateral-PNP transistor is shown in Fig. 10.3. The base-to-emitter voltage applied to this device establishes the per-unit-length current density that flows in a direction perpendicular to the emitter. The relative currents intercepted by the two collectors are thus equal to the relative collector lengths. The concept can be extended, and lateral-PNP transistors with three or more collectors are used in some designs.

One advantage of the lateral-PNP structure is that the base-to-emitter breakdown voltage of this device is equal to the collector-to-base breakdown voltage of the NPN transistors that are formed by the same process. This feature permits nonlinear operation with large different input voltages for operational amplifiers that include lateral PNP's in their input stage. (Two examples are given in Section 10.4.)

A second possible PNP structure is the vertical or substrate PNP illustrated in Fig. 10.4. This type of transistor consists of an emitter formed by the NPN base diffusion and a base of NPN collector material, with the substrate forming the *P*-type collector. The base width is the difference between the depth of the *P*-type diffusion and the thickness of the epitaxial layer and can be controlled moderately well. Current gain can be reasonably high and

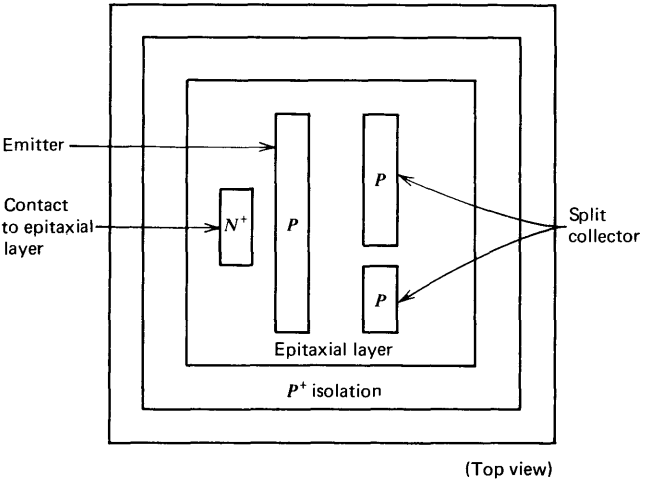


Figure 10.3 Split-collector lateral-PNP transistor.

bandwidth is considerably better than that of a lateral design. One undesirable consequence of the necessary compromises is that large-area transistors must be used to maintain gain at moderate current levels. Another more serious difficulty is that the collectors of all substrate PNP's are common and are connected to the negative supply voltage. Thus substrate PNP's can only be used as emitter followers.

10.2.3 Other Components

The *P*-type base material is normally used for resistors, and the resistivity of this material dictated by the base-region doping level is typically 100 to 200 ohms per square. Problems associated with achieving high length-to-width ratios in a reasonable area and with tolerable distributed capacitance usually limit maximum resistance values to the order of 10 kilo-ohms. Similarly, other geometric considerations limit the lower value of resistors

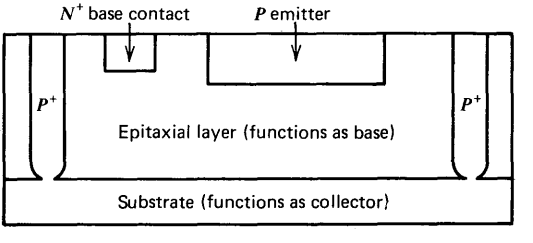


Figure 10.4 Vertical or substrate PNP transistor.

made using the base diffusion to the order of 25 ohms. Higher-value resistors (up to approximately 100 kilo-ohms) can be made using the higher-resistivity collector material, while lower-value resistors are formed from the heavily doped emitter material.

Practical considerations make control of absolute resistance values to better than 10 to 20% uneconomical, and the temperature coefficient of all integrated-circuit resistors is high by discrete-component standards. However, it is possible to match two resistors to 5% or better, and all resistors made from one diffusion have identical temperature coefficients.

It is possible to make large-value, small-geometry resistors by diffusing emitter material across a base-material resistor (see Fig. 10.5). The cross-sectional area of the current path is decreased by this diffusion, and resistance values on the order of 10 kΩ per square are possible. The resultant device, called a pinched resistor, has the highly nonlinear characteristics illustrated in Fig. 10.6. The lower-current portion of this curve results from field-effect transistor action, with the *P*-type resistor material forming a channel surrounded by an *N*-type gate. The potential of the gate region is maintained close to that of the most positive end of the channel by conduction through the *P*-*N* junction. Thus, if the positively biased end of the pinched resistor is considered the source of a *P*-channel FET, the characteristics of the resistor are the drain characteristics of a FET with approximately zero gate-to-source voltage. When the voltage applied across the structure exceeds the reverse breakdown voltage of the N^+ and *P* junction, the heavily doped N^+ region forms a low-resistance path across the resistor. The high-conductance region of the characteristics results from this effect.

In addition to the nonlinearity described above, the absolute value of a pinched resistor is considerably harder to control than that of a standard base-region resistor. In spite of these limitations, pinched resistors are used

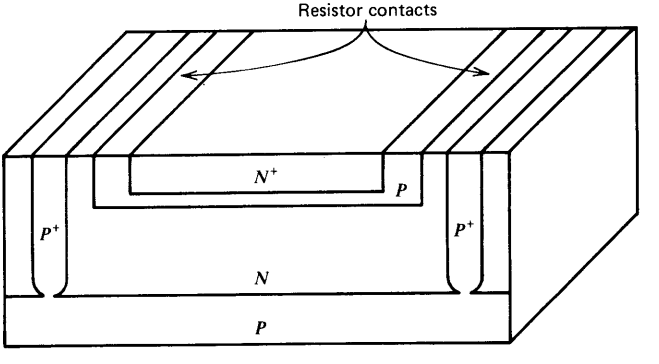


Figure 10.5 Pinched resistor.

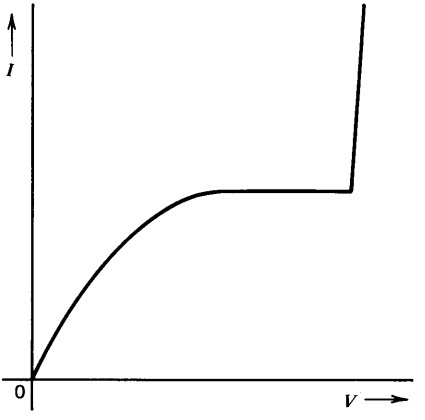


Figure 10.6 Pinched-resistor current-voltage characteristic.

in integrated circuits, often as shunt paths across base-to-emitter junctions of bipolar transistors. The absolute value of such a shunt path is relatively unimportant in many designs, and the voltage applied to the resistor is limited to a fraction of a volt by the transistor junction.

An alternative high-resistance structure that has been used as a bias current source in some integrated-circuit designs is the collector FET shown in Fig. 10.7. This device, which acts as an *N*-channel FET with its gate biased at the negative supply voltage of circuit, does not have the breakdown-voltage problems associated with the pinched resistor.

Integrated-circuit diodes are readily fabricated. The collector-to-base junction of NPN transistors can be used when moderately high reverse breakdown voltage is necessary. The diode-connected transistor (Fig. 10.8) is used when diode characteristics matched to transistor characteristics are required. If it is assumed that the transistor terminal relationships are

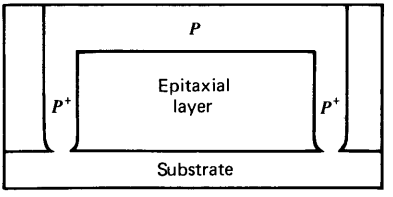
$$I_C = I_S \, e^{qV_{BE}/kT}$$

we can write for the diode-connected transistor

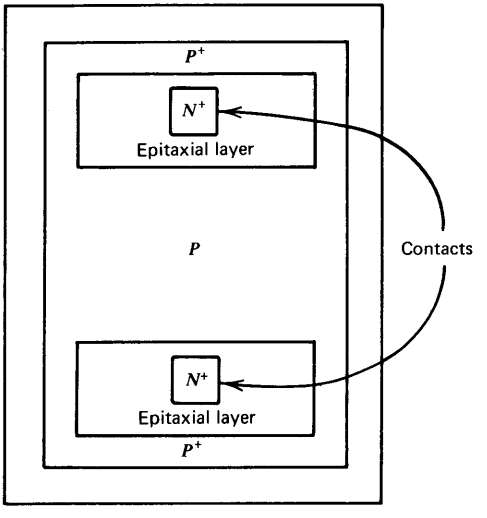
$$I_D = I_B + I_C = \left(1 + \frac{1}{\beta}\right) I_C$$

$$= \left(1 + \frac{1}{\beta}\right) I_S \, e^{qV_D/kT} \simeq I_S \, e^{qV_D/kT} \qquad (10.1)$$

The base-to-emitter junction is used as a Zener diode in some circuits. The reverse breakdown voltage of this junction is determined by transistor processing, with a typical value of six volts.



(a)



(b)

Figure 10.7 Collector FET. (*a*) Cross-section view. (*b*) Top view.

Reverse-biased diode junctions can be used as capacitors when the nonlinear characteristics of the space-charge-layer capacitance are acceptable. An alternative linear capacitor structure uses the oxide as a dielectric, with the aluminum metalization layer one plate and the semiconductor material the second plate. This type of metal-oxide-semiconductor capacitor has the further advantage of bipolar operation compared with a diode. The capacitance per unit area of either of these structures makes capacitors larger than 100 pF impractical.

10.3 INTEGRATED-CIRCUIT DESIGN TECHNIQUES

Most high-volume manufacturers of integrated circuits have chosen to live with the limitations of the six-mask process in order to enjoy the

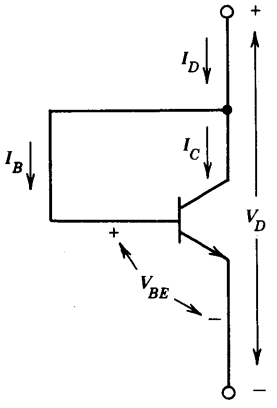


Figure 10.8 Diode-connected transistor.

associated economy. This process dictates circuit considerations beyond those implied by the limited spectrum of component types. For example, large-value base-material resistors or capacitors require a disproportionate share of the total chip area of a circuit. Since defects occur with a per-unit-area probability, the use of larger areas that decrease the yield of the process and thus increase production cost are to be avoided.

The designers of integrated operational amplifiers try to make maximum use of the advantages of integrated processing such as the large number of transistors that can be economically included in each circuit and the excellent match and thermal equality that can be achieved among various components in order to circumvent its limitations. The remarkable performance of presently available designs is a tribute to their success in achieving this objective. This section describes some of the circuit configurations that have evolved from this type of design effort.

10.3.1 Current Repeaters

Many linear integrated circuits use a connection similar to that shown in Fig. 10.9, either for biasing or as a controlled current source. Assume that both transistors have identical values for saturation current I_S and that β is high so that base currents of both transistors can be neglected. In this case, the collector current of Q_1 is equal to i_I. Since the base-to-emitter voltages of Q_1 and Q_2 are identical, currents i_I and i_O must be equal.[4] An

[4] In the discussion of this and other current-repeater connections it is assumed that the output terminal voltage is such that the output transistor is in its forward operating region. Note that it is not necessary to have the driving current i_I supplied from a current source. In many actual designs, this current is supplied from a voltage source via a resistor or from another active device.

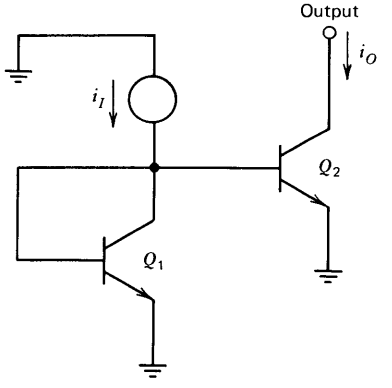


Figure 10.9 Current repeater.

alternative is to change the relative areas of Q_1 and Q_2. This geometric change results in a directly proportional change in saturation currents, so that currents i_I and i_O become a controlled multiple of each other. If i_I is made constant, transistor Q_2 functions as a current source for voltages to within approximately 100 mV of ground. This performance permits the dynamic voltage range of many designs to be nearly equal to the supply voltage.

The split-collector lateral PNP transistor described earlier functions as a current repeater when connected as shown in Fig. 10.10. The constant K that relates the two collector currents in this connection depends on the relative sizes of the collector segments. Since the base current for the

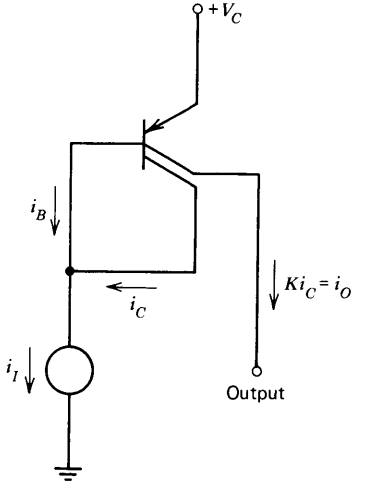


Figure 10.10 Split-collector PNP transistor connected for controlled gain.

lateral PNP is equal to the sum of the two collector currents divided by its current gain β_P, we can write

$$i_I = i_B + i_C = i_C \frac{(1 + K)}{\beta_P} + i_C \tag{10.2}$$

and

$$i_O = K i_C \tag{10.3}$$

Combining Eqns. 10.2 and 10.3 shows that the current gain for this connection is

$$\frac{i_O}{i_I} = \frac{K}{1 + [(1 + K)/\beta_P]} \tag{10.4}$$

If values are selected so that $1 + K \ll \beta_P$, the feedback inherent to this connection makes its input-output transfer ratio relatively insensitive to changes in β_P. This desensitivity is advantageous since the quantity K, determined by mask geometry, is significantly better controlled than is β_P. The feedback also increases the current-gain half-power frequency of the controlled-gain PNP above the β cutoff frequency of the lateral-PNP transistor itself.

The simple current repeater shown in Fig. 10.9 is frequently augmented to make its current transfer ratio less sensitive to changes in transistor parameters. Equal-value emitter resistors can be included to stabilize the transfer ratio of the connection for changes in the base-to-emitter voltages of the two transistors. While this technique is sometimes used for discrete-component current repeaters, it is of questionable value in many integrated designs because matched resistors are as difficult to fabricate as matched transistors.

Other modifications are intended to reduce the dependency of the current transfer ratio on the transistor current gain. It is easily shown that the current transfer ratio for Fig. 10.9, assuming perfectly matched transistors, is

$$\frac{i_O}{i_I} = \frac{1}{1 + 2/\beta} \tag{10.5}$$

Figure 10.11 shows two somewhat more complex current-repeater connections assumed constructed with perfectly matched transistors. Intermediate currents that facilitate calculation of current transfer ratios are included in these diagrams. The circuit of Fig. 10.11*a* uses an emitter follower to buffer the base currents of a conventional current repeater. The resultant current transfer ratio is

$$\frac{i_O}{i_I} = \frac{1}{1 + 2/[\beta(\beta + 1)]} = \frac{\beta^2 + \beta}{\beta^2 + \beta + 2} \tag{10.6}$$

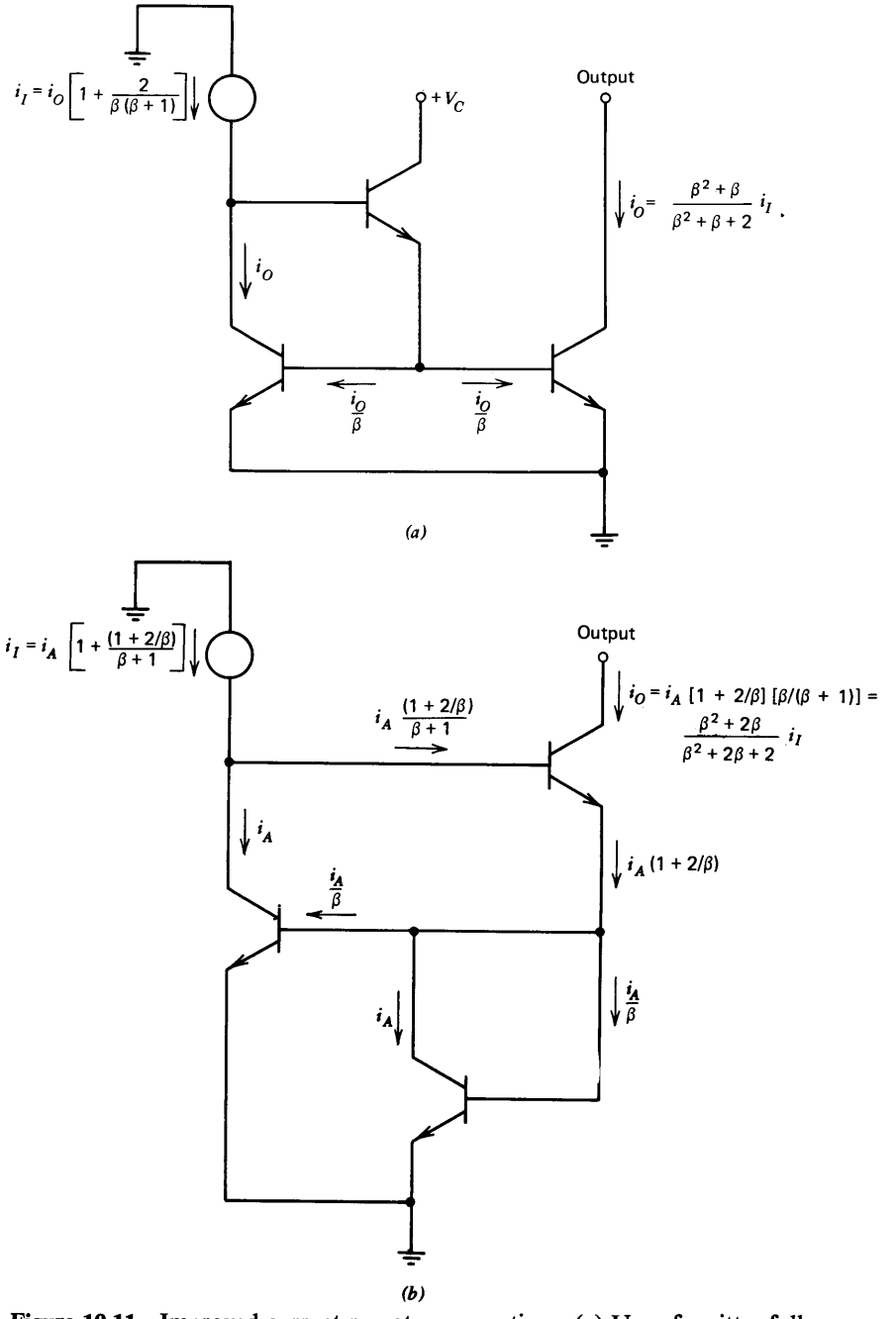


Figure 10.11 Improved current-repeater connections. (*a*) Use of emitter follower. (*b*) Use of current compensation.

The connection of Fig. 10.11*b* uses an interesting current cancellation technique to obtain a transfer ratio

$$\frac{i_O}{i_I} = \frac{[1 + 2/\beta]\ [\beta/(\beta + 1)]}{1 + (1 + 2/\beta)/(\beta + 1)} = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} \tag{10.7}$$

Either of these currents repeaters has a transfer ratio that differs from unity by a factor of approximately $(1 + 2/\beta^2)$ compared with a factor of $(1 + 2/\beta)$ for the circuit of Fig. 10.9, and are thus considerably less sensitive to variations in β. It can also be shown (see Problem P10.5) that the output resistance of the circuit illustrated in Fig. 10.11*b* is the order of $r\mu$ while that of either of the other circuits is the order of r_o. This difference is significant in some high-gain connections.

A clever modification of the current repeater, first used in the 709 design, yields a low-value constant-current source using only moderate-value resistors. Assuming high β and a large value of V relative to V_{BE1} in Fig. 10.12,

$$I_{C1} \simeq \frac{V}{R_1} \tag{10.8}$$

so that

$$V_{BE1} \simeq \frac{kT}{q} \ln \frac{V}{R_1 I_{S1}} \tag{10.9}$$

However,

$$I_{C2}R_2 + \frac{kT}{q} \ln \frac{I_{C2}}{I_{S2}} = V_{BE1} \tag{10.10}$$

If it is assumed that saturation currents are equal, combining Eqns. 10.9 and 10.10 yields

$$I_{C2}R_2 = \frac{kT}{q} \ln \frac{V}{R_1 I_{C2}} \tag{10.11}$$

The resultant transcendental equation can be solved for any particular choice of constants. For example, if Eqn. 10.11 is evaluated at room temperature ($kT/q \simeq 26$ mV) for $V/R_1 = 1$ mA and $R_2 = 12$ kΩ, $I_{C2} \simeq 10\ \mu$A.

10.3.2 Other Connections

Most operational-amplifier designs require both NPN and PNP transistors in order to provide voltage level shifting. Several connections effectively augment the low gain of many lateral PNP designs by combining the PNP transistor with an NPN transistor as shown in Fig. 10.13. (This connection is also used in discrete-component circuits and is called the *complementary*

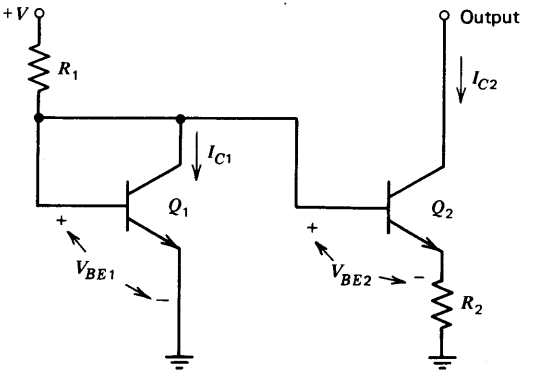


Figure 10.12 Low-level current source.

Darlington connection.) At low frequencies this combination appears as a single PNP transistor with the base, emitter, and collector terminals as indicated. The current gain of this compound transistor is approximately equal to the product of the gains of the two individual devices, while transconductance is related to collector current of the combination as in a conventional transistor.

An ingenious connection using lateral PNP transistors, shown in Fig. 10.14, was introduced in the LM101 amplifier design. Assume that the two NPN transistors have identical saturation currents, as do the PNP's. Further assume that the current gains of both PNP transistors are β_P. The total output collector current, $i_{C3} + i_{C4}$, must be equal to $\beta_P I$. If the input voltages

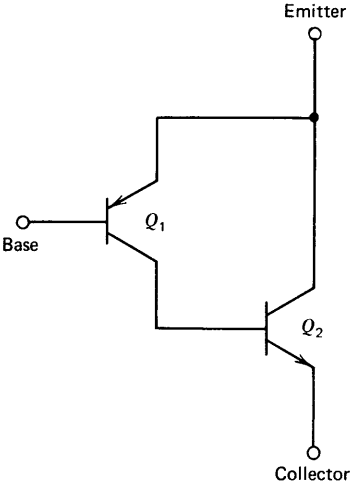


Figure 10.13 Complementary Darlington connection.

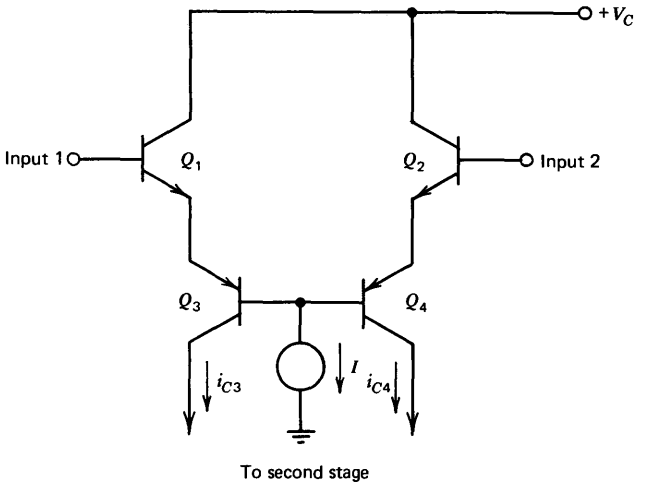


Figure 10.14 Differential input stage.

are equal, i_{C3} and i_{C4} must be equal because of the matched saturation currents. As a differential input signal is applied, the relative collector currents change differentially; therefore this stage can be used to perform the circuit function of a differential pair of PNP transistors. However, the ratio of input current to collector current depends on the current gain of the high-gain NPN's. Another advantage is that the input capacitance is low since the input transistors are operating as emitter followers. Furthermore, the low-bandwidth PNP devices are operating in an incrementally grounded-base connection for differential input signals, and this connection maximizes their bandwidth in the circuit. One disadvantage is that the series connection of four base-to-emitter junctions lowers transconductance by a factor of two compared to a standard differential amplifier operating at the same quiescent current level.

It is interesting to note that the successful operation of this circuit is actually dependent on the low gain characteristic of the lateral-PNP transistors used. If high-gain transistors were used, capacitive loading at the bases of the two PNP transistors would cause large collector currents as a function of the time rate of change of common-mode level. The controlled gain PNP shown in Fig. 10.10 is used in this connection in some modern amplifier designs.

Several connections are used to double the effective transconductance of an input differential pair and thus increase the gain provided by this portion of an operational amplifier. One such circuit is shown in Fig. 10.15. Assume equal operating currents for Q_1 and Q_2. If Q_4 were a constant

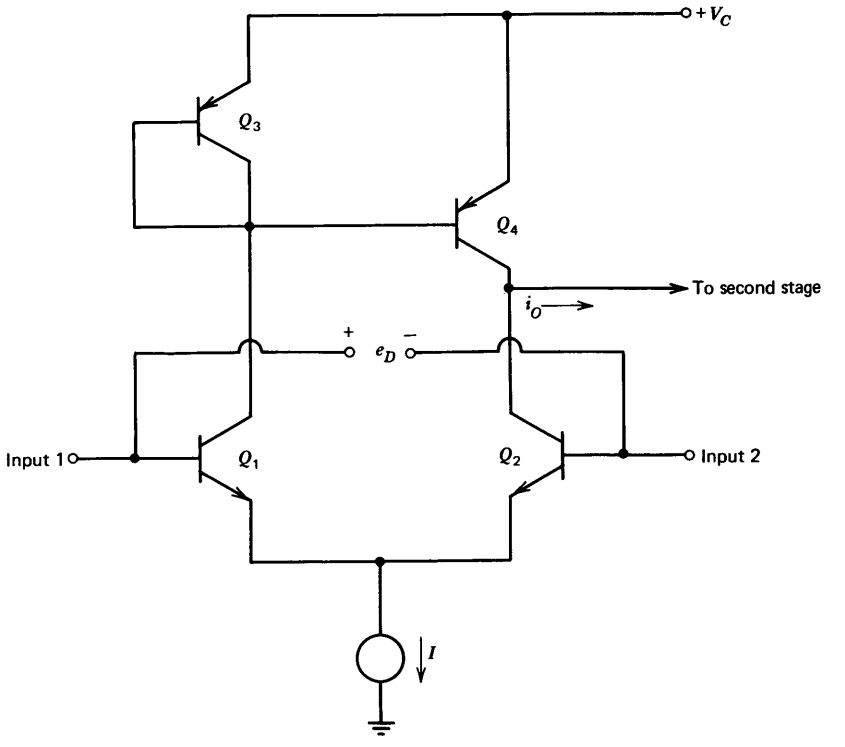


Figure 10.15 Use of current repeater to increase stage transconductance.

current source, the incremental output current would be related to a differential input voltage e_d as $i_o/e_d = g_m/2$. The differential connection of Q_1 and Q_2 insures that incremental changes in collector currents of these devices are equal in magnitude but opposite in polarity, and the current repeater connection of Q_3 and Q_4 effectively subtracts the change in collector current of Q_1 from that of Q_2. (The more sophisticated current repeaters described in the last section are often substituted.) The gain is increased by a factor of two so that $i_o/e_d = g_m$. Another advantage is that the impedance level at the circuit output is high so that this stage can provide high voltage gain if required. We will see that some integrated-circuit operational amplifiers exploit this possibility to distribute the total gain more equally between the two stages than was done with the discrete-component design discussed in the last chapter.

Another approach is illustrated in Fig. 10.16. A differential input causes equal-magnitude changes in the collector currents of Q_1 and Q_2. However, the high gain of the Q_3-Q_5 loop changes the voltage at the emitter of Q_5 in

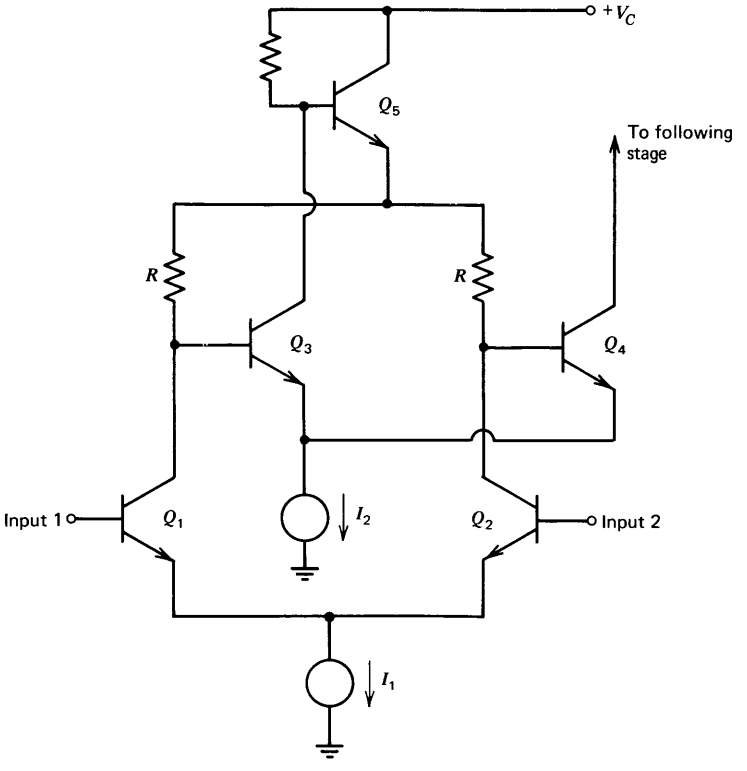


Figure 10.16 Use of local feedback to increase stage transconductance.

such a way as to minimize current changes at the base of Q_3. Thus the current through the load resistor for Q_1 is changed by an amount approximately equal to the change in i_{C1}. A corresponding change occurs in the current through the load resistor for Q_2, doubling the current into the base of Q_4.

10.4 REPRESENTATIVE INTEGRATED-CIRCUIT OPERATIONAL AMPLIFIERS

A number of semiconductor manufacturers presently offer a variety of integrated-circuit operational amplifiers. While an exhaustive study of available amplifiers is beyond the scope of this book, an examination of several representative designs demonstrates some of the possible variations of the basic topology described in Chapters 8 and 9 and serves as a useful prelude to the material on applications.

It should be mentioned that most of the circuits described are popular enough to be built, often with minor modifications, by a number of manufacturers. These "second-source" designs usually retain a designation that maintains an association with the original. Another factor that contributes to the proliferation of part numbers is that most manufacturers divide their production runs into two or three categories on the basis of measured parameters such as input bias current and offset voltage as well as the temperature range over which specifications are guaranteed. For example, National Semiconductor uses the 100, 200, and 300 series to designate whether military, intermediate, or commercial temperature range specifications are met, while Fairchild presently suffixes a C to designate commercial temperature range devices.

We should observe that no guarantee of inferior performance is implied when the less splendidly specified devices are used. Since all devices in one family are made by an identical process and since yields are constantly improving, a logical conclusion is that many commercially specified devices must in fact be meeting military specifications. These considerations coupled with a dramatic cost advantage (the order of a factor of three) suggest the use of the commercial devices in all but the most exacting applications.

10.4.1 The LM101 and LM101A Operational Amplifiers

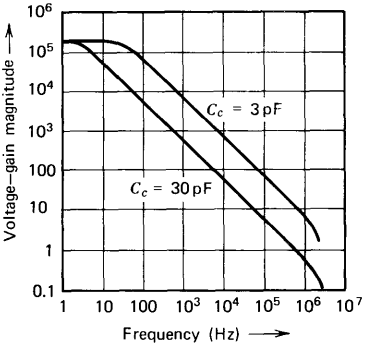
The LM101 operational amplifier[5] occupies an important place in the history of integrated-circuit amplifiers since it was the first design to use the two-stage topology combined with minor-loop feedback for compensation. Its superiority was such that it stimulated a variety of competing designs as well as serving as the ancestor of several more advanced National Semiconductor amplifiers.

The schematic diagram for the amplifier is shown in Fig. 10.17, and specifications are included in Table 10.1. (The definitions of some of the specified quantities are given in Chapter 11.) As was the case with the discrete-component amplifier described in the last chapter, it is first necessary to identify the functions of the various transistors, with emphasis placed on the transistors in the gain path. Transistors Q_1 through Q_4 form a differential input connection as described in the last section. The Q_5 through Q_7 triad is a current-repeater load for the differential stage. Transistors Q_8 and Q_9 are connected as an emitter follower driving a high voltage gain common-emitter stage. The voltage gains of the first and second stages

[5] R. J. Widlar, "A New Monolithic Operational Amplifier Design," National Semiconductor Corporation, Technical Paper TP-2, June, 1967.

Table 10.1 LM101 Specifications: Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Input offset voltage	$T_A = 25°$ C, $R_S \leq 10$ kΩ		1.0	5.0	mV
Input offset current	$T_A = 25°$ C		40	200	nA
Input bias current	$T_A = 25°$ C		120	500	nA
Input resistance	$T_A = 25°$ C	300	800		kΩ
Supply current	$T_A = 25°$ C, $V_S = \pm 20$ V		1.8	3.0	mA
Large-signal voltage gain	$T_A = 25°$ C, $V_S = \pm 15$ V				
	$V_{out} = \pm 10$ V, $R_L \geq 2$ kΩ	50	160		V/mV
Input offset voltage	$R_S \leq 10$ kΩ			6.0	mV
Average temperature coefficient of input offset voltage	$R_S \leq 50$ Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Input offset current	$T_A = +125°$ C		10	200	nA
	$T_A = -55°$ C		100	500	nA
Input bias current	$T_A = -55°$ C		0.28	1.5	μA
Supply current	$T_A = +125°$ C, $V_S = \pm 20$ V		1.2	2.5	mA
Large-signal voltage gain	$V_S = \pm 15$ V, $V_{out} = \pm 10$ V				
	$R_L \geq 2$ kΩ	25			V/mV
Output voltage swing	$V_S = \pm 15$ V, $R_L = 10$ kΩ	±12	±14		V
	$R_L = 2$ kΩ	±10	±13		V
Input voltage range	$V_S = \pm 15$ V	±12			V
Common-mode rejection ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply-voltage rejection ratio	$R_S \leq 10$ kΩ	70	90		dB



Open – loop freqnency response
±15 – volt supplies, 25°C

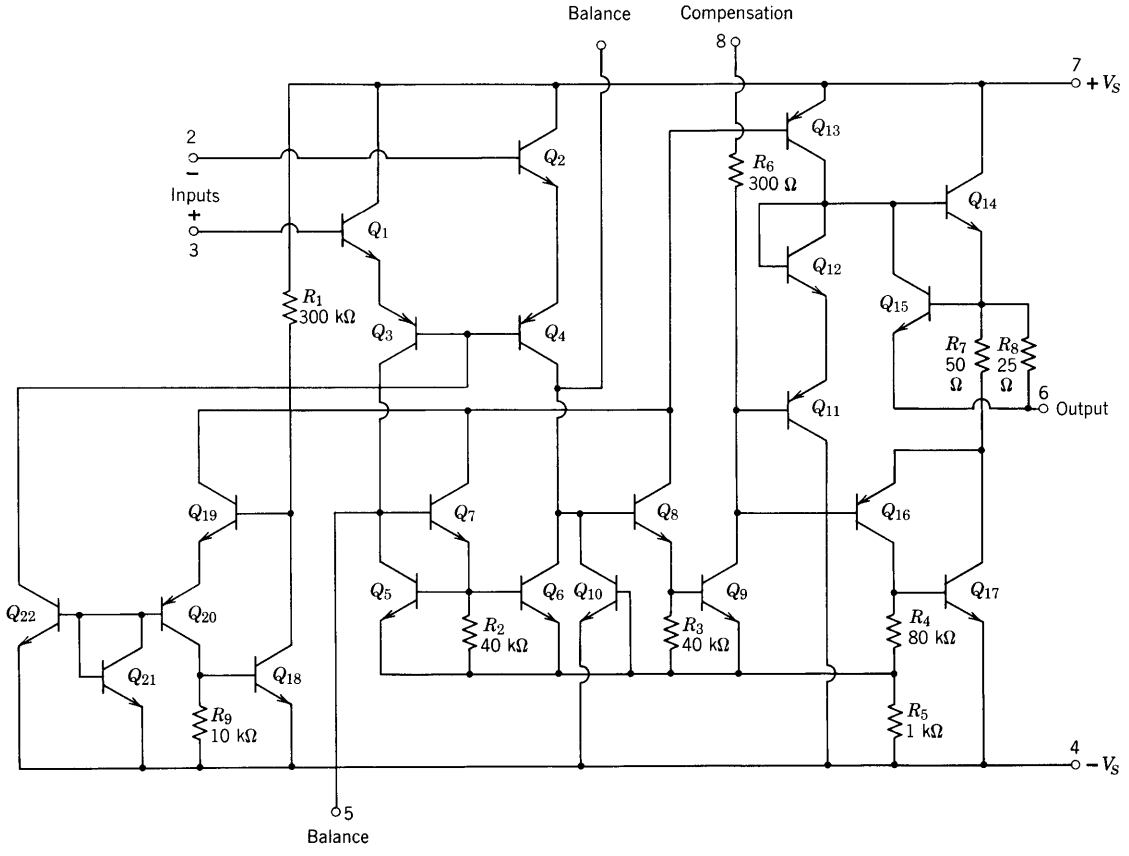


Figure 10.17 LM101 schematic diagram.

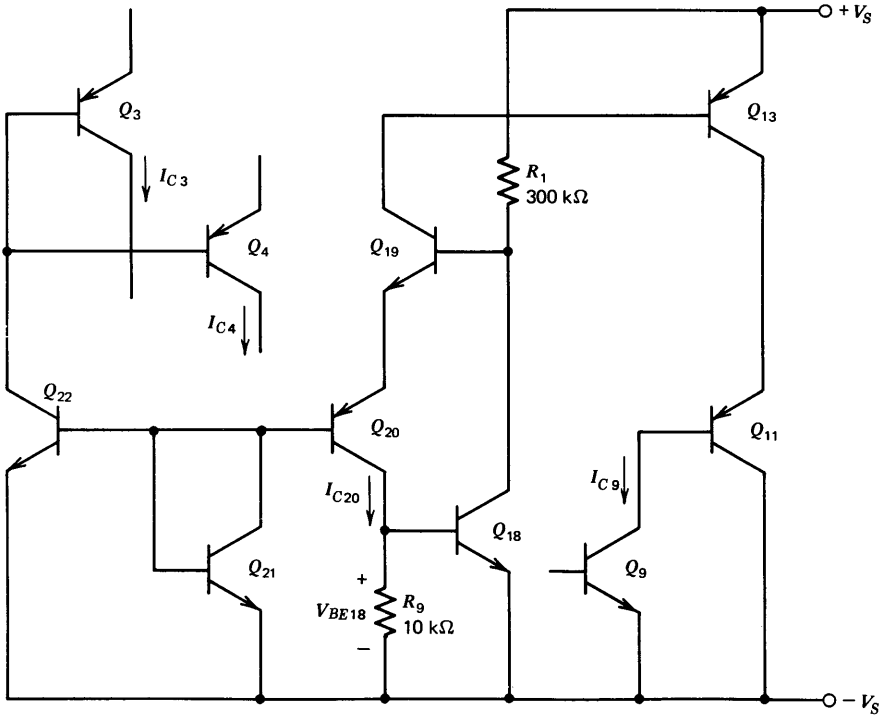


Figure 10.18 LM101 bias circuitry.

of this amplifier are both proportional to the reciprocal of the base-width modulation factor and thus are comparable in magnitude.

The complementary Darlington connection Q_{16} and Q_{17} supplies negative output current. The use of this connection augments the low gain of the lateral PNP. (Recall that this amplifier was manufactured when current gains of 5 to 10 were anticipated from lateral-PNP transistors.) While a vertical-PNP transistor could have been used in the output stage, the designer of the 101 elected the complementary Darlington since it reduced total chip area[6] and since processing was simplified.

Positive output current is supplied by Q_{14}. The gain path from the collector of Q_9 to the emitter of Q_{14} includes transistor Q_{11}, another lateral PNP. This device matches the current gain from the collector of Q_9 to the output for positive output swings with the gain for negative output swings. By locating current source Q_{13} in the emitter circuit of Q_{11}, this current source provides bias for Q_{11} as well as a high-resistance load for Q_9. Diode-

[6] It is interesting to note that the size of the LM101 chip is 0.045 inch square, smaller than many single transistors.

connected transistor Q_{12} is included in the output circuit to reduce cross-over distortion.

The operation of the biasing circuit for the LM101 depends on achieving equal current gains from certain lateral-PNP transistors. This approach was used since while low, unpredictable gains characterized the lateral PNP's of the era, the performance was highly uniform from device to device on one chip. The transistors used for biasing are shown in Fig. 10.18. The loop containing transistors Q_{18}, Q_{19}, and Q_{20} controls I_{C20} so that $I_{C20} \simeq V_{BE18}/R_9 \simeq 60\ \mu A$.

The high-value resistor, R_1, included in this circuit is a collector FET. The characteristics of this resistor make the current supplied by it relatively independent of supply voltage. The base current of Q_{20} is repeated by transistors Q_{21} and Q_{22} and applied to the common-base connection of Q_3 and Q_4. If the areas of Q_{21} and Q_{22} and the current gains of Q_3, Q_4, and Q_{20} were equal, the total first-stage collector current, $I_{C3} + I_{C4}$, would be equal to I_{C20}. The area of Q_{21} is actually made larger than that of Q_{22} so that each input transistor operates at a quiescent collector current of 10 μA.

Biasing for transistor Q_9 includes transistors Q_{11}, Q_{13}, Q_{19}, and Q_{20}. Assuming high gain from Q_{19},

$$I_{C9} = \frac{I_{C20}(\beta_{20} + 1)}{\beta_{20}} \frac{\beta_{13}}{(1 + \beta_{11})} \tag{10.12}$$

Thus $I_{C9} = I_{C20}$ for equal PNP gains.

The actual circuit (Fig. 10.17) shows that the collectors of Q_7 and Q_8 are connected in parallel with that of Q_{19}. This doesn't significantly alter operation since $I_{C19} \gg I_{C7} \simeq I_{C8}$, and allows a smaller geometry chip since Q_7, Q_8, and Q_{19} can all be located in the same isolation diffusion.

Positive output current is limited by transistor Q_{15} (Fig. 10.17) when the voltage across R_8 becomes approximately 0.6 volt. The negative current limit is more involved. When the voltage across R_7 reaches approximately 1.2 volts, the collector-to-base junction of Q_{15} becomes forward biased, and further increases in output current are supplied by Q_{11}. Since this lateral PNP has low gain, the emitter current of Q_9 increases significantly when the limiting value of output current is reached. The emitter current of Q_9 flows through R_5, and when the drop across this resistor reaches 0.6 volt, transistor Q_{10} limits base drive for Q_8, preventing further increases in output current.

There are two reasons for this unusual limiting circuit. First, the peculiarities of lateral PNP Q_{16} make it advantageous to have relatively high resistance between the emitter of this transistor and the output of the circuit to insure stability with capacitive loads. Second, this limit also protects Q_9 if its collector is clamped to some voltage level. Such clamping applied to point 8 can be used to limit the output voltage of the amplifier.

The amplifier can be balanced to reduce input offset voltage by connecting a high-value resistor (typically 20 MΩ to 100 MΩ) from either point 5 or point 1 to ground. This type of balancing results in minimum voltage drift from the input transistors.

Compensating minor-loop feedback around the high-gain portion of the circuit is applied between points 1 to 8. The 300-Ω resistor in this circuit provides a zero at a frequency approximately one decade above the amplifier unity-gain frequency when a capacitor is used for compensation. The positive phase shift associated with this zero improves amplifier stability.

Measurements made on the amplifier show that the transconductance from the input terminals to the base of Q_8 is approximately 2×10^{-4} mho so that the open-loop transfer function of the amplifier at frequencies of interest is approximately $2 \times 10^{-4}/Y_c$, where Y_c is the short-circuit transfer admittance of the compensating network as defined in Section 9.2.3. This value of transconductance is consistent with the four series-connected input transistors operating at 10 μA of quiescent current. The transconductance to either output of the differential pair is $qI_C/4kT \simeq 10^{-4}$ mho, and this value is doubled by the current-repeater load used for the input stage. While the compensating network does load the high-impedance node at the collector of Q_9, such loading is usually insignificant.

The open-loop transfer function included as part of the specifications shows that the amplifier has a single-pole response with a unity-gain frequency of approximately 1 MHz when compensated with a 30-pF capacitor. This result can also be obtained from the analytic expression given above. The amplifier dynamics other than those which result from the inner loop limit the crossover frequency of loops using this amplifier to between 1 and 2 MHz. The phase shift that leads to instability for higher crossover frequencies results primarily from the lateral PNP transistors in the input stage.

Evolutionary modifications changed the LM101 amplifier to the LM101A shown in Fig. 10.19, and this amplifier is (as of this writing) still the standard to which all other general-purpose, externally compensated integrated operational amplifiers are compared. The differences reflect primarily the increased performance of components available at the time the LM101A was designed. Better matching tolerances reduced the maximum input offset voltage to 2 mV at 25° C and improved common-mode rejection ratio and power-supply rejection modestly. Improved input-transistor current gain and a modified bias circuit reduced the maximum input bias current over the full −55° C to +125° C temperature range to 100 nA and reduced the typical room-temperature offset current to 1.5 nA.

A detailed discussion of the bias circuit of the LM101A (transistors Q_{18} through Q_{22} in Fig. 10.19) is beyond the scope of the book.[7] Its most im-

[7] R. J. Widlar, "I. C. Op Amp with Improved Input-Current Characteristics," *EEE*, pp. 38–41, December, 1968.

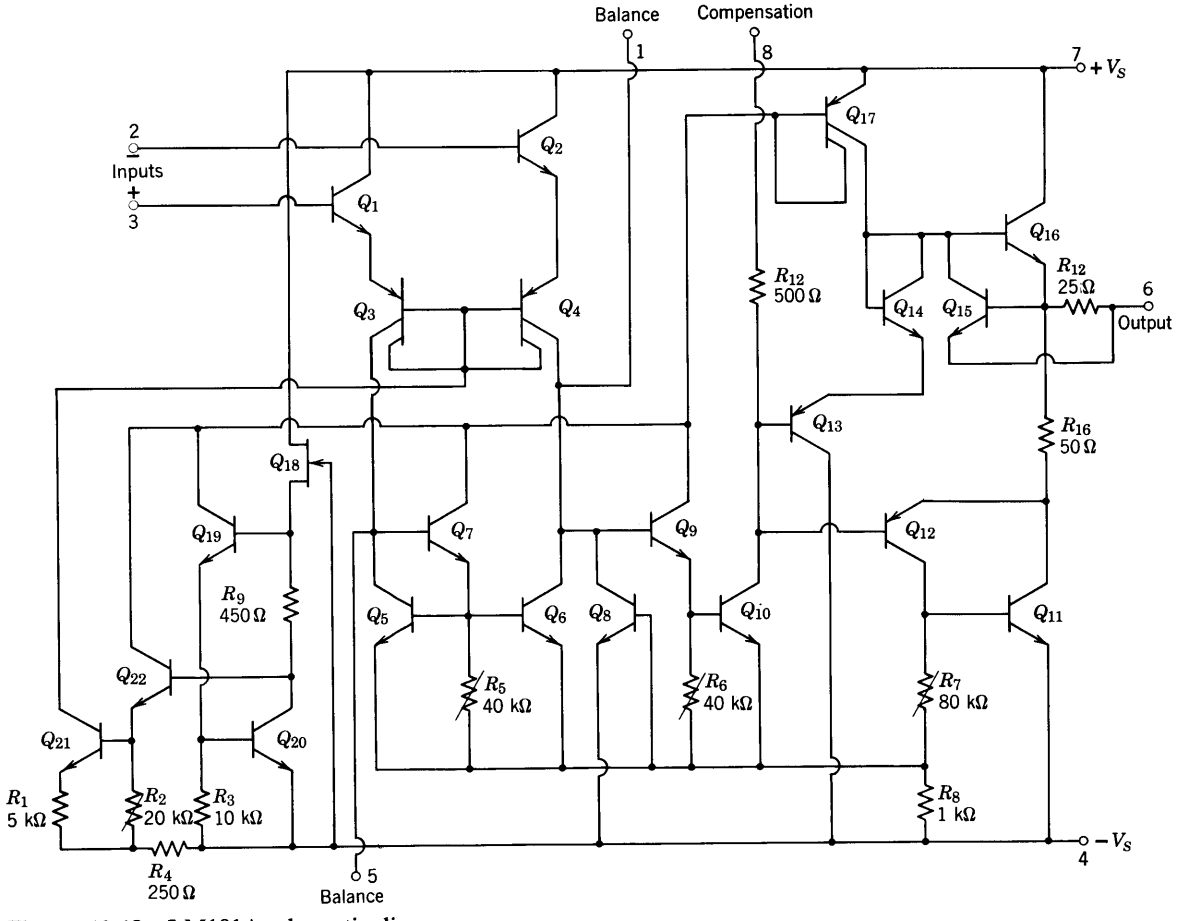


Figure. 10.19 LM101A schematic diagram.

Table 10.2 μA776 Specifications: $\pm$15 Volt Operation for 776; Electrical Characteristics (T_A is 25° C, unless otherwise specified)

Parameter		Conditions	I_{SET} = 1.5 μA Min	Typ	Max	I_{SET} = 15 μA Min	Typ	Max	Units
Input offset voltage		$R_S \leq 10$ kΩ		2.0	5.0		2.0	5.0	mV
Input offset current				0.7	3.0		2.0	15	nA
Input bias current				2.0	7.5		15	50	nA
Input resistance				50			5.0		MΩ
Input capacitance				2.0			2.0		pF
Offset voltage adjustment range				9.0			18		mV
Large-signal voltage gain		$R_L \geq 75$ kΩ, $V_{out} = \pm 10$ V	200	400					V/mV
		$R_L \geq 5$ kΩ, $V_{out} = \pm 10$ V				100	400		V/mV
Output resistance				5.0			1.0		kΩ
Output short-circuit current				3.0			12		mA
Supply current				20	25		160	180	μA
Power consumption					0.75			5.4	mW
Transient response (unity gain)	Rise time	$V_{in} = 20$ mV, $R_L \geq 5$ kΩ, $C_L = 100$ pF		1.6			0.35		μs
	Overshoot			0			10		%
Slew rate		$R_L \geq 5$ kΩ		0.1			0.8		V/μs
Output voltage swing		$R_L \geq 75$ kΩ	± 12	± 14					V
		$R_L \geq 5$ kΩ				± 10	± 13		V

The following specifications apply: $-55°\ C \leq T_A \leq +125°\ C$

Input offset voltage	$R_S \leq 10\ k\Omega$			6.0			6.0	mV
Input offset current	$T_A = +125°\ C$			5.0			15	nA
	$T_A = -55°\ C$			10			40	nA
Input bias current	$T_A = +125°\ C$			7.5			50	nA
	$T_A = -55°\ C$			20			120	nA
Input-voltage range		±10			±10			V
Common-mode rejection ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply-voltage rejection ratio	$R_S \leq 10\ k\Omega$		25	150		25	150	μV/V
Large-signal voltage gain	$R_L \geq 75\ k\Omega$, $V_{out} = \pm 10\ V$	100			75			V/mV
Output voltage swing	$R_L \geq 75\ k\Omega$	±10			±10			V
Supply current				30			200	μA
Power consumption				0.9			6.0	mW

portant functional characteristic is that the quiescent collector current of the input stage is made proportional to absolute temperature. As a result, the transconductance of the input stage (which has a direct effect on the compensated open-loop transfer function of the amplifier) is made virtually temperature independent. A subsidiary benefit is that the change in quiescent current with temperature partially offsets the current-gain change of the input transistors so that the temperature dependence of the input bias current is reduced. The modified bias circuit became practical because the improved gain stability of the controlled-gain lateral PNP's used in the LM101A eliminated the requirement for the bias circuit to compensate for gross variations in lateral-PNP gain.

We shall get a greater appreciation for the versatility of the LM101A, particularly with respect to the control of its dynamics afforded by various types of compensation, in Chapter 13.

10.4.2 The μA776 Operational Amplifier

The LM101A circuit described in the previous section can be tailored for use in a variety of applications by choice of compensation. An interesting alternative way of modifying amplifier performance by changing its quiescent operating currents is used in the μA776 operational amplifier. Some of the tradeoffs that result from quiescent current changes were discussed in Section 9.3.3, and we recall that lower operating currents compromise bandwidth in exchange for reduced input bias current and power consumption.

The schematic diagram for this amplifier is shown in Fig. 10.20, with performance specifications listed in Table 10.2. Several topological similarities between this amplifier and the LM101 are evident. Transistors Q_1 through Q_6 form a current-repeater-loaded differential input stage. Transistors Q_7 and Q_9 are an emitter-follower common-emitter combination loaded by current source Q_{12}. Diode-connected transistors Q_{21} and Q_{22} forward bias the Q_{10}-Q_{11} complementary output pair. Capacitor C_1 compensates the amplifier.

The unique feature of the μA776 is that all quiescent operating currents are referenced to the current labeled I_{SET} in the schematic diagram by means of a series of current repeaters. Thus changing this set current causes proportional changes in all quiescent currents and scales the current-dependent amplifier parameters.

The collector current of Q_{19} is proportional to the set current because of the Q_{16}-Q_{18}-Q_{19} connection. The difference between this current and the collector current of Q_{15} is applied to the common-base connection of the Q_3-Q_4 pair. The collector current of Q_{15} is proportional to the total quiescent operating current of the differential input stage, since Q_{14} and Q_{15} form a current repeater for the sum of the collector currents of Q_1 and Q_2.

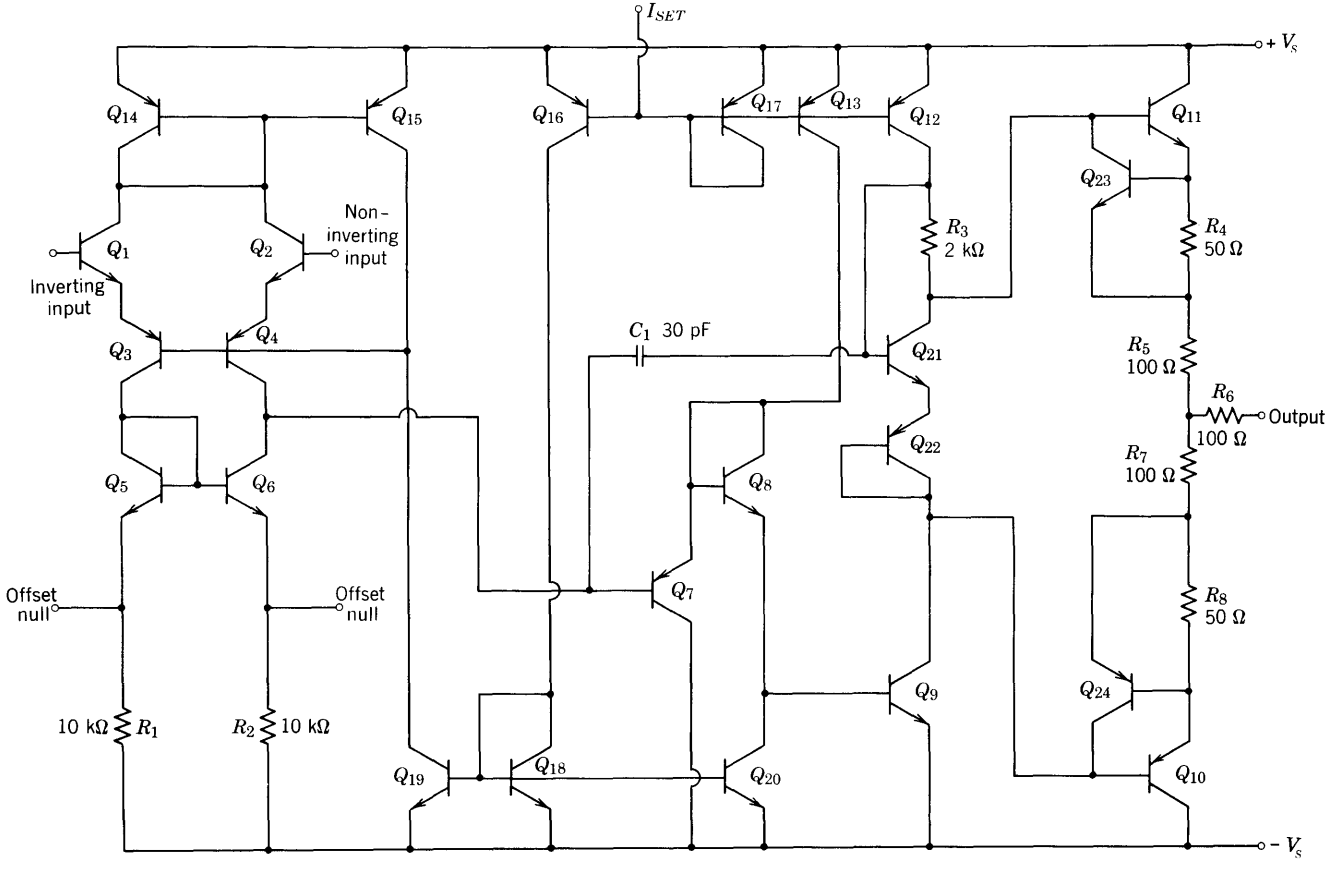


Figure 10.20 μA776 schematic diagram.

The resultant negative feedback loop stabilizes quiescent differential-stage current. The geometries of the various transistors are such that the quiescent collector currents of Q_1, Q_2, Q_3, and Q_4 are each approximately equal to I_{SET}.

The amplifier can be balanced by changing the relative values of the emitter resistors of the Q_5-Q_6 current-repeater pair via an external potentiometer. While this balance method does not equalize the base-to-emitter voltages of the Q_5-Q_6 pair, any drift increase is minimal because of the excellent match of first-stage components. An advantage is that the external balance terminals connect to low-impedance circuit points making the amplifier less susceptible to externally-generated noise.

One of the design objectives for the μA776 was to make input- and output-voltage dynamic ranges close to the supply voltages so that low-voltage operation became practical. For this purpose, the vertical PNP Q_7 is used as the emitter-follower portion of the high-gain stage. The quiescent voltage at the base of Q_7 is approximately the same as the voltage at the base of Q_9 (one diode potential above the negative supply voltage) since the base-to-emitter voltage of Q_7 and the forward voltage of diode-connected transistor Q_8 are comparable. (Current sources Q_{13} and Q_{20} bias Q_7 and Q_8.) Because the operating potential of Q_7 is close to the negative supply, the input stage remains linear for common-mode voltages within about 1.5 volts of the negative supply.

Transistor Q_{21} is a modified diode-connected transistor which, in conjunction with Q_{22}, reduces output stage crossover distortion. At low set-current levels (resulting in correspondingly low collector currents for Q_9 and Q_{12}) the drop across R_3 is negligible, and the potential applied between the bases of Q_{10} and Q_{11} is equal to the sum of the base-to-emitter voltages of Q_{21} and Q_{22}. At higher set currents, the voltage drop across R_3 lowers the ratio of output-stage quiescent current to that of Q_9 as an aid toward maintaining low power consumption.

A vertical-PNP transistor is used in the complementary output stage, and this stage, combined with its driver (Q_9 and Q_{12}), permits an output voltage dynamic range within approximately one volt of the supplies at low output currents. Current limiting is identical to that used in the discrete-component amplifier described in Chapter 9.

The ability to change operating currents lends itself to rather interesting applications. For example, operation with input bias currents in the picoampere region and power consumption at the nanowatt level is possible with appropriately low set current if low bandwidth is tolerable. The amplifier can also effectively be turned into an open circuit at its input and output terminals by making the set current zero, and thus can be used as an analog switch. Since the unity-gain frequency for this amplifier is $g_m/(2 \times 30\ \text{pF})$

where g_m is the (assumed equal) transconductance of transistors Q_1 through Q_4, changes in operating current result in directly proportional changes in unity-gain frequency.

This amplifier is inherently a low-power device, even at modest set-current levels. For example, many performance specifications for a μA776 operating at a set current of 10 μA are comparable to those of an LM101A when compensated with a 30-pF capacitor. However, the power consumption of the μA776 is approximately 3 mW at this set current (assuming operation from 15-volt supplies) while that of the LM101A is 50 mW. The difference reflects the fact that the operating currents of the second and output stage are comparable to that of the first stage in the μA776, while higher relative currents are used in the LM101A. One reason that this difference is possible is that the slew rate of the μA776 is limited by its fixed, 30-pF compensating capacitor. Higher second-stage current is necessary in the LM101A to allow higher slew rates when alternate compensating networks are used.

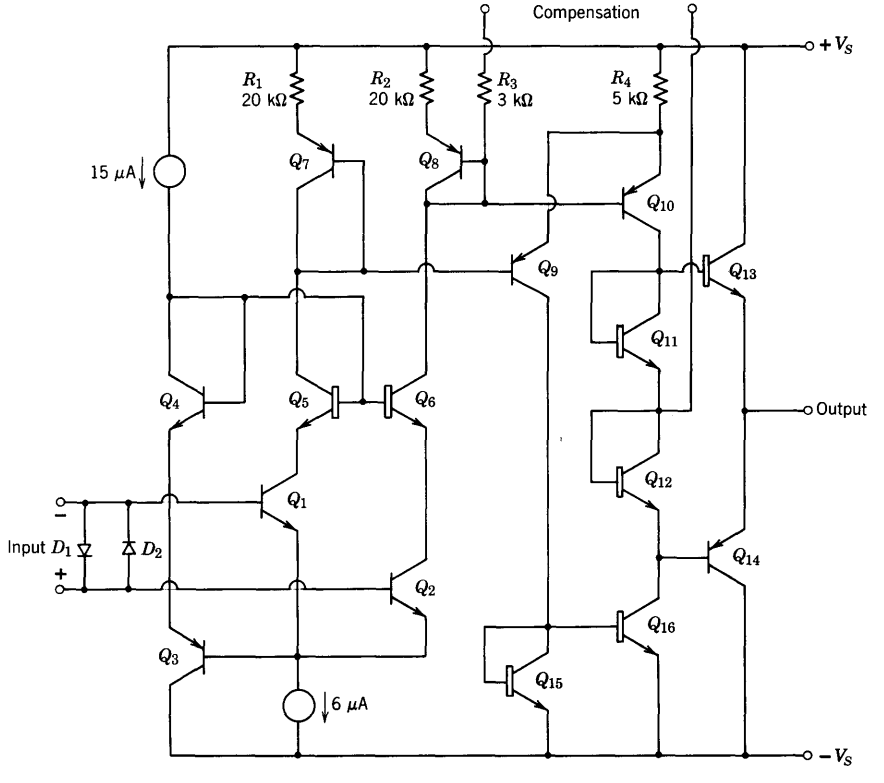


Figure 10.21 LM108 simplified schematic diagram.

Table 10.3 LM108 Specifications: Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Input offset voltage	$T_A = 25°$ C		0.7	2.0	mV
Input offset current	$T_A = 25°$ C		0.05	0.2	nA
Input bias current	$T_A = 25°$ C		0.8	2.0	nA
Input resistance	$T_A = 25°$ C	30	70		MΩ
Supply current	$T_A = 25°$ C		0.3	0.6	mA
Large-signal voltage gain	$T_A = 25°$ C, $V_S = \pm 15$ V				
	$V_{out} = \pm 10$ V, $R_L \geq 10$ kΩ	50	300		V/mV
Input offset voltage				3.0	mV
Average temperature coefficient of input-offset voltage			3.0	15	μV/°C
Input offset current				0.4	nA
Average temperature coefficient of input offset current			0.5	2.5	pA/°C
Input bias current				3.0	nA
Supply current	$T_A = +125°$ C		0.15	0.4	mA
Large-signal voltage gain	$V_S = \pm 15$ V, $V_{out} = \pm 10$ V				
	$R_L \geq 10$ kΩ	25			V/mV
Output voltage swing	$V_S = \pm 15$ V, $R_L = 10$ kΩ	±13	±14		V
Input voltage range	$V_S = \pm 15$ V	±14			V
Common-mode rejection ratio		85	100		dB
Supply-voltage rejection ratio		80	96		dB

10.4.3 The LM108 Operational Amplifier[8]

The LM108 operational amplifier was the first general-purpose design to use super β transistors in order to achieve ultra-low input currents. While a detailed discussion of the operation of this circuit is beyond the scope of this book, the LM108 does illustrate another of the many useful ways that the basic two-stage topology can be realized.

A simplified schematic diagram that illustrates some of the more important features of the design is shown in Fig. 10.21, with specifications given in Table 10.3. (The complete circuit, which is considerably more complex, is described in the reference given in the footnote.) The schematic diagram indicates two types of NPN transistors. Those with a narrow base (Q_1, Q_2, and Q_4) are super β transistors with current gains of several thousand and low breakdown voltage. The wide-base NPN transistors are conventional devices.

The input differential pair operates at a quiescent current level of 3 μA per device. This quiescent level combined with the high gain of Q_1 and Q_2 results in an input bias current of less than one nanoampere, and thus the LM108 is ideally suited to use in high-impedance circuits.

In order to prevent voltage breakdown of the input transistors, their collectors are bootstrapped via cascode transistors Q_5 and Q_6. Operating currents and geometries of transistors Q_3, Q_4, Q_5, and Q_6 are chosen so that the input transistors operate at nearly zero collector-to-base voltage. Thus collector-to-base leakage current (which can dominate input current at elevated temperatures) is largely eliminated. It is also necessary to diode clamp the input terminals to prevent breaking down input transistors under large-signal conditions. This clamping, which deteriorates performance in some nonlinear applications, is one of the prices paid for low input current.

Transistors Q_9 and Q_{10} form a second-stage differential amplifier. Diode-connected transistors Q_7 and Q_8 compensate for the base-to-emitter voltages of Q_9-Q_{10}, so that the quiescent voltage across R_4 is equal to that across R_1 or R_2. Resistor values are such that second-stage quiescent current is twice that of the first stage. Transistors Q_{15} and Q_{16} connected as a current repeater reflect the collector current of Q_9 as a load for Q_{10}. This connection doubles the voltage gain of the second stage compared with using a fixed-magnitude current source as the load for Q_{10}. The high-resistance node is buffered with a conventional output stage.

Compensation can be effected by forming an inner loop via collector-to-base feedback around Q_{10}. Circuit parameters are such that single-pole compensation with dynamics comparable to the feedback-compensated case results when a dominant pole is created by shunting a capacitor from

[8] R. J. Widlar, "I. C. Op Amp Beats FET's on Input Current," National Semiconductor Corporation, Application note AN-29, December, 1969.

the high-resistance node to ground. This alternate compensation results in superior supply-voltage noise rejection. (One disadvantage of capacitive coupling from collector to base of a second-stage transistor is that this feedback forces the transistor to couple high-frequency supply-voltage transients applied to its emitter directly to the amplifier output.)

The dynamics of the LM108 are not as good as those of the LM101A. While comparable bandwidths are possible in low-gain, resistively loaded applications, the bandwidth of the LM101A is substantially better when high closed-loop voltage gain or capacitive loading is required. The slower dynamics of the LM108 result in part from the use of the lateral PNP's in the second stage where their peculiarities more directly affect bandwidth and partially from the low quiescent currents used to reduce the power consumption of the circuit by a factor of five compared with that of the LM101A.

10.4.4 The LM110 Voltage Follower

The three amplifiers described earlier in this section have been general-purpose operational amplifiers where one design objective was to insure that the circuit could be used in a wide variety of applications. If this requirement is relaxed, the resultant topological freedom can at times be

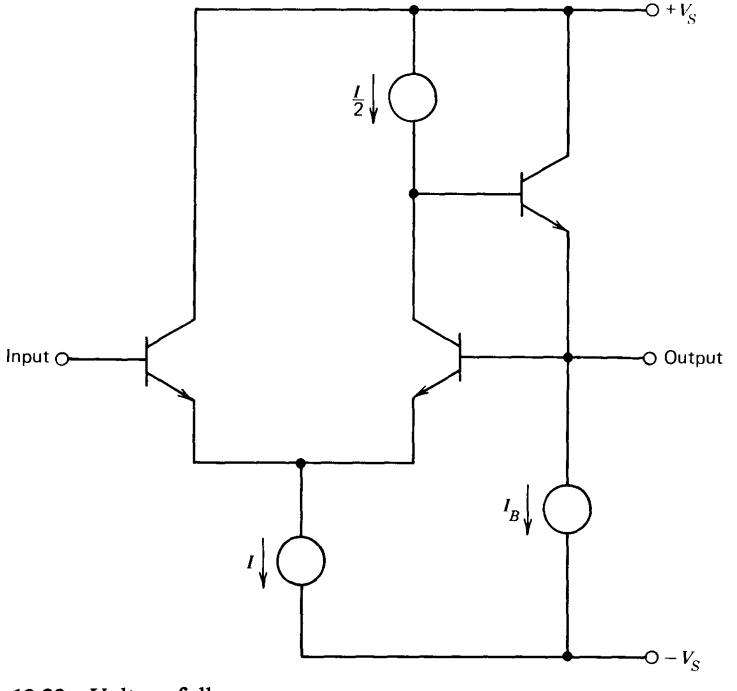


Figure 10.22 Voltage follower.

exploited. Consider the simplified amplifier shown in Fig. 10.22. Here a current-source-loaded differential amplifier is used as a single high-gain stage and is buffered by an emitter follower. The emitter follower is biased with a current source. This very simple operational amplifier is connected in a unity-gain noninverting or voltage-follower configuration. Since it is known that the input and output voltage levels are equal under normal operating conditions, there is no need to allow for arbitrary input-output voltage relationships. One very significant advantage is that only NPN transistors are included in the gain path, and the bandwidth limitations that result from lateral PNP transistors are eliminated.

This topology is actually a one-stage amplifier, and the dynamics associated with such designs are even more impressive than those of two-stage amplifiers. While the low-frequency open-loop voltage gain of this design may be less than that of two-stage amplifiers, open-loop voltage gains of several thousand result in adequate desensitivity when direct output-to-input feedback is used.

The LM110 voltage follower (Fig.10-23) is an integrated-circuit operational amplifier that elaborates on the one-stage topology described above. Perfomance specifications are listed in Table 10.4. Note that this circuit, like the LM108, uses both super β (narrow base) and conventional (wide base) NPN transistors. The input stage consists of transistors Q_8 through Q_{11} connected as a differential amplifier using two modified Darlington pairs. Pinch resistors R_8 and R_9 increase the emitter current of Q_8 and Q_{11} to reduce voltage drift. (See Section 7.4.4 for a discussion of the drift that can result from a conventional Darlington connection.) Transistor Q_{15} supplies the operating current for the input stage. Transistor Q_{16} supplies one-half of this current (the nominal operating current of either side of the differential pair) to the current repeater Q_1 through Q_3 that functions as the first-stage load.

Transistors Q_5 and Q_6 form a Darlington emitter follower that isolates the high-resistance node from loads applied to the amplifier. The emitter of Q_6, which is at approximately the output voltage, is used to bootstrap the collector voltage of the Q_{10}-Q_{11} pair. The resultant operation at nominally zero collector-to-base voltage results in negligible leakage current from Q_{11}. The Q_8-Q_9 pair is cascoded with transistor Q_4. Besides protecting Q_8 and Q_9 from excessive voltages, the cascode results in higher open-loop voltage gain from the circuit.

Diode D_1 and diode-connected transistor Q_{13} limit the input-to-output voltage difference for a large-signal operation to protect the super β transistors and to speed overload recovery. Transistor Q_7 is a current limiter, while Q_{14} functions as a current-source load for the output stage. The single-ended emitter follower is used in preference to a complementary

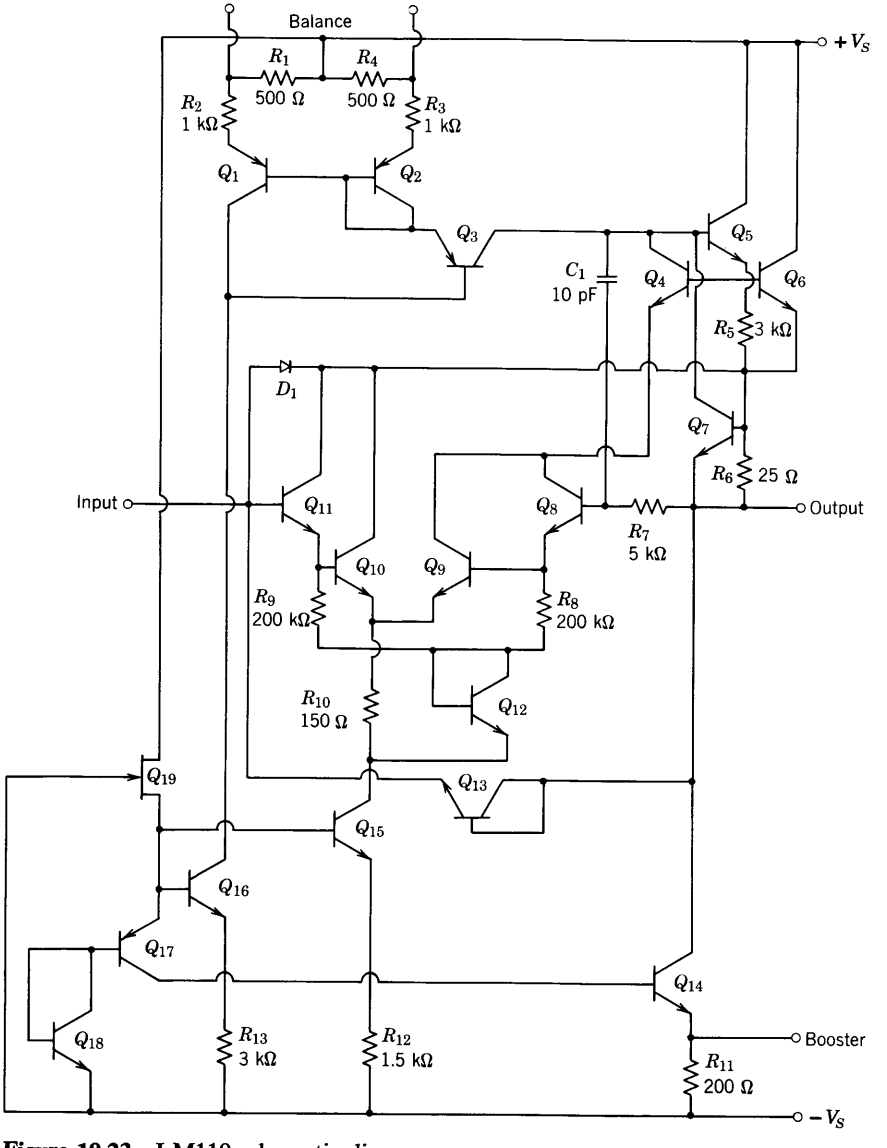


Figure 10.23 LM110 schematic diagram.

Table 10.4 LM110 Specifications: Electrical Characteristics

Parameter	Conditions	Min	Typ.	Max	Units
Input offset voltage	$T_A = 25°$ C		1.5	4.0	mV
Input bias current	$T_A = 25°$ C		1.0	3.0	nA
Input resistance	$T_A = 25°$ C	10^{10}	10^{12}		Ω
Input capacitance			1.5		pF
Large-signal voltage gain	$T_A = 25°$ C, $V_S = \pm 15$ V				
	$V_{out} = \pm 10$ V, $R_L = 8$ kΩ	0.999	0.9999		V/V
Output resistance	$T_A = 25°$ C		0.75	2.5	Ω
Supply current	$T_A = 25°$ C		3.9	5.5	mA
Input offset voltage				6.0	mV
Offset voltage	$-55° \text{ C} \leq T_A \leq 85°$ C		6		μV/°C
temperature drift	$T_A = 125°$ C		12		μV/°C
Input bias current				10	nA
Large-signal voltage gain	$V_S = \pm 15$ V, $V_{out} = \pm 10$ V				
	$R_L = 10$ kΩ	0.999			V/V
Output voltage swing	$V_S = \pm 15$ V, $R_L = 10$ kΩ	±10			V
Supply current	$T_A = 125°$ C		2.0	4.0	mA
Supply-voltage rejection ratio	$5 \text{ V} \leq V_S \leq 18$ V	70	80		dB

connection since it is more linear and thus better suited to high-frequency applications. An interesting feature of the design is that the magnitude of the current-source load for the emitter follower can be increased by shunting resistor R_{11} via external terminals. This current can be increased when it is necessary for the amplifier to supply substantial negative output current. The use of boosted output current also increases the power consumption of the circuit, raises its temperature, and can reduce input current because of the increased current gain of transistor Q_{11} at elevated temperatures.

The capacitive feedback from the collector of Q_4 to the base of Q_8 stabilizes the amplifier. Since the relative potentials are constrained under normal operating conditions, a diode can be used for the capacitor.

The small-signal bandwidth of the LM110 is approximately 20 MHz. This bandwidth is possible from an amplifier produced by the six-mask process because, while lateral PNP's are used for biasing or as static current sources, none are used in the signal path.

It is clear that special designs to improve performance can often be employed if the intended applications of an amplifier are constrained. Unfortunately, most special-purpose designs have such limited utility that fabrication in integrated-circuit form is not economically feasible. The LM110 is an example of a circuit for which such a special design is practical, and it provides significant performance advantages compared to general-purpose amplifiers connected as followers.

10.4.5 Recent Developments

The creativity of the designers of integrated circuits in general and monolithic operational amplifiers in particular seems far from depleted. Innovations in processing and circuit design that permit improved performance occur with satisfying regularity. In this section some of the more promising recent developments that may presage exciting future trends are described.

The maximum closed-loop bandwidth of most general-purpose monolithic operational amplifiers made by the six-mark process is limited to approximately 1 MHz by the phase shift associated with the lateral-PNP transistors used for level shifting. While this bandwidth is more than adequate for many applications, and in fact is advantageous in some because amplifiers of modest bandwidth are significantly more tolerant of poor decoupling, sloppy layout, capacitive loading, and other indiscretions than are faster designs, wider bandwidth always extends the application spectrum. Since it is questionable if dramatic improvements will be made in the frequency response of process-compatible PNP transistors in the near future, present efforts to extend amplifier bandwidth focus on eliminating the lateral PNP's from the gain path, at least at high frequencies.

One possibility is to capacitively bypass the lateral PNP's at high frequencies. This modification can be made to an LM101 or LM101A by connecting a capacitor from the inverting input to terminal 1 (see Figs. 10.17 and 10.19). The capacitor provides a feedforward path (see Section 8.2.2) that bypasses the input-stage PNP transistors. Closed-loop bandwidths on the order of 5 MHz are possible, and this method of compensation is discussed in greater detail in a later section. Unfortunately, feedforward does not improve the amplifier speed for signals applied to the noninverting input, and as a result wideband differential operation is not possible.

The LM118 pioneered a useful variation on this theme. This operational amplifier is a three-stage design including an NPN differential input stage, an intermediate stage of lateral PNP's that provides level shifting, and a final NPN voltage-gain stage. The intermediate stage is capacitively bypassed, so that feedforward around the lateral-PNP stage converts the circuit to a two-stage NPN design at high frequencies, while the PNP stage provides the gain and level shifting required at low frequencies. Since the feedforward is used following the input stage, full bandwidth differential operation is retained. Internal compensation insures stability with direct feedback from the output to the inverting input and results in a unity-gain frequency of approximately 15 MHz and a slew rate of at least 50 volts per microsecond. External compensation can be used for greater relative stability.

A second possibility is to use the voltage drop that a current source produces across a resistor for level shifting. It is interesting to note that the μA702, the first monolithic operational amplifier that was designed before the advent of lateral PNP's, uses this technique and is capable of closed-loop bandwidths in excess of 20 MHz. However, the other performance specifications of this amplifier preclude its use in demanding applications. The μA715 is a more modern amplifier that uses this method of level shifting. It is an externally compensated amplifier capable of a closed-loop bandwidth of approximately 20 MHz and a slew rate of 100 V/μs in some connections.

It is evident that improved high-speed amplifiers will evolve in the future. The low-cost availability of these designs will encourage the use of circuits such as the high-speed digital-to-analog converters that incorporate them.

A host of possible monolithic operational-amplifier refinements may stem from improved thermal design. One problem is that many presently available amplifiers have a d-c gain that is limited by thermal feedback on the chip. Consider, for example, an amplifier with a d-c open-loop gain of 10^5, so that the input differential voltage required for a 10-volt output is 100 μV. If the thermal gradient that results from the 10-volt change in output level changes the input-transistor pair temperature differentially

by 0.05° C (a real possibility, particularly if the output is loaded), differential input voltage is dominated by thermal feedback rather than by limited d-c gain. Several modern instrumentation amplifiers use sophisticated thermal-design techniques such as multiple, parallel-connected input transistors located to average thermal gradients and thus allow usable gains in the range of 10^6. These techniques should be incorporated into general-purpose operational amplifiers in the future.

An interesting method of output-transistor protection was originally developed for several monolithic voltage regulators, and has been included in the design of at least one high-power monolithic operational amplifier. The level at which output current should be limited in order to protect a circuit is a complex function of output voltage, supply voltage, the heat sink used, ambient temperature, and the time history of these quantities because of the thermal dynamics of the circuit. Any limit based only on output current level (as is true with most presently available operational amplifiers) must be necessarily conservative to insure protection. An attractive alternative is to monitor the temperature of the chip and to cut off the output before this temperature reaches destructive levels. As this technique is incorporated in more operational-amplifier designs, both output current capability and safety (certain present amplifiers fail when the output is shorted to a supply voltage) will improve. The high pulsed-current capability made possible by thermal protection would be particularly valuable in applications where high-transient capacitive changing currents are encountered, such as sample-and-hold circuits.

Another thermal-design possibility is to include temperature sensors and heaters on the chip so that its temperature can be stabilized at a level above the highest anticipated ambient value. This technique has been used in the μA726 differential pair and μA727 differential amplifier. Its inclusion in a general-purpose operational-amplifier design would make parameters such as input current and offset independent of ambient temperature fluctuations.

10.5 ADDITIONS TO IMPROVE PERFORMANCE

Operational amplifiers are usually designed for general-purpose applicability. For this reason and because of limitations inherent to integrated-circuit fabrication, the combination of an integrated-circuit operational amplifier with a few discrete components often tailors performance advantageously for certain applications. The use of customized compensation networks gives the designer a powerful technique for modifying the dynamics of externally compensated operational amplifiers. This topic is discussed in Chapter 13. Other frequently used modifications are intended to improve either the input-stage or the output-stage characteristics of

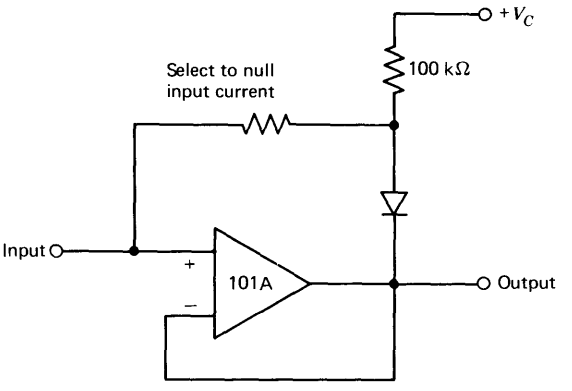


Figure 10.24 Input current compensation for voltage follower.

monolithic amplifiers, and some of these additions are mentioned in this section.

One advantage that many discrete-component operational amplifiers have compared with some integrated-circuit designs is lower input current. This improvement usually results because the input current of the discrete-component design is compensated by one of the techniques described in Section 7.4.2. These techniques can reduce the input current of discrete-component designs, particularly at one temperature, to very low levels. The same techniques can be used to lower the input current of integrated-circuit amplifiers. Many amplifiers can be well compensated using transistors as shown in Fig. 7.14. Transistor types, such as the 2N4250 or 2N3799, which have current-gain versus temperature characteristics similar to those of the input transistors of many amplifiers, should be used.

The connection shown in Fig. 10.24 can be used to reduce the input current of a follower-connected LM101A. As a consequence of the temperature-dependent input-stage operating current of this amplifier (see Section 10.4.1), the temperature coefficient of its input current is approximately 0.3% per degree Centigrade, comparable to that of a forward-biased silicon diode at room temperature.

Another possibility involves the use of the low input current LM110 as a preamplifier for an operational amplifier. Since the bandwidth of the LM110 is much greater than that of most general-purpose operational amplifiers, feedback-loop dynamics are unaffected by the addition of the preamplifier. While this connection increases voltage drift, the use of self heating (see Section 10.4.4) and simple input current compensation can result in an input current under 0.5 nA over a wide temperature range.[9]

[9] While the LM108 has comparably low input current, its dynamics and load-driving capability are inferior to those of many other general-purpose amplifiers. As a result the connection described here is advantageous in some applications.

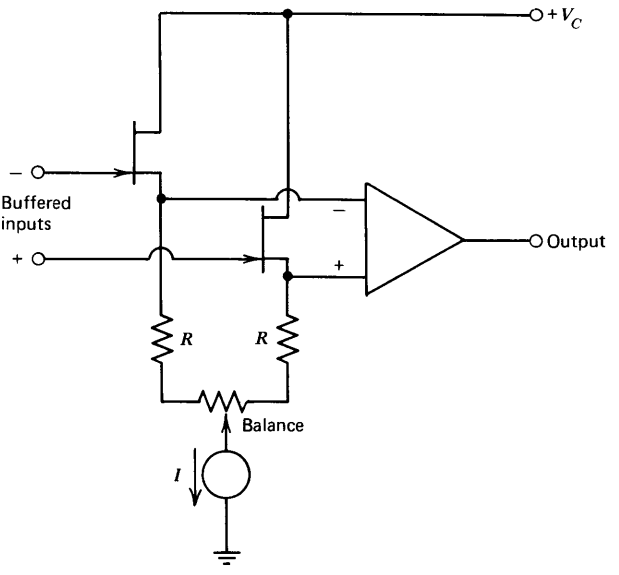


Figure 10.25 Use of FET followers.

Field-effect transistors[10] can be connected as source followers in front of an operational amplifier as shown in Fig. 10.25. Input current of a fraction of a nA at moderate temperatures is obtained at the expense of increased drift and poorer common-mode rejection ratio. The use of relatively inexpensive dual field-effect transistors yields typical drift figures of 10 to 100 μV/°C. The product of source-follower output resistance and amplifier input capacitance is normally small enough so that dynamics remain unchanged. If this capacitive loading is a problem, the gate and source terminals of the FET's can be shunted with small capacitors.

It is possible to reduce the drift of an operational amplifier by preceding it with a differential-amplifier stage, since the drift of a properly designed discrete-component differential amplifier can be made a fraction of a microvolt per degree Centigrade (see Chapter 7). This method is most effective when relatively high voltage gain is obtained from the differential stage and when its operating current is high compared with the input

[10] While the best-matched field-effect transistors are made by a monolithic process, the process cannot simultaneously fabricate high-quality bipolar transistors. Some manufacturers offer hybrid integrated circuits that combine two chips in one package to provide a FET-input operational amplifier. The μA740 is a monolithic FET-input amplifier, but its performance is not as good as that of the hybrids.

current of the operational amplifier. A recently developed integrated circuit (the LM121) is also intended to function as a preamplifier for operational amplifiers. The bias current of this preamplifier can be adjusted, and combined drift of less than one microvolt per degree Centigrade is possible. The use of a preamplifier that provides voltage gain often complicates compensation because the increased loop transmission that results may compromise stability in some applications.

The output current obtainable from an integrated-circuit operational amplifier is limited by the relatively small geometry of the output transistors and by the low power dissipation of a small chip. These limitations can be overcome by following the amplifier with a separate output stage.

There is a further significant performance advantage associated with the use of an external output stage. If output current is supplied from a transistor included on the chip, the dominant chip power dissipation is that associated with load current when currents in excess of several milliamperes are supplied. As a consequence, chip temperature can be strongly dependent on output voltage level. As mentioned earlier, thermal feedback to the input transistors deteriorates performance because of associated drift and input current changes. A properly designed output stage can isolate the amplifier from changes in load current so that chip temperature becomes virtually independent of output voltage and current.

Output-stage designs of the type described in Section 8.4 can be used. The wide bandwidth of emitter-follower circuits normally does not compromise frequency response. The output stage can be a discrete-component design, or any of several monolithic or hydrid integrated circuits may be used. The MC1538R is an example of a monolithic circuit that can be used as a unity-gain output buffer for an operational amplifier. This circuit is housed in a relatively large package that permits substantial power dissipation, and can provide output currents as high as 300 mA. Its bandwidth exceeds 8 MHz, considerably greater than that of most general-purpose operational amplifiers.

Another possibility in low output power situations is to use a second operational amplifier connected as a noninverting amplifier (gains between 10 and 100 are commonly used) as an output stage for a preceding operational amplifier. Advantages include the open-loop gain increase provided by the noninverting amplifier, and virtual elimination of thermal-feedback problems since the maximum output voltage required from the first amplifier is the maximum output voltage of the combination divided by the closed-loop gain of the noninverting amplifier. It is frequently necessary to compensate the first amplifier very conservatively to maintain stability in feedback loops that use this combination.

PROBLEMS

P10.1

You are the president of Single-Stone Semiconductor, Inc. Your best-selling product is a general-purpose operational amplifier that has chip dimensions of 0.05 inch square. Experience shows that you make a satisfactory profit if you sell your circuits at a price equal to 10 times the cost at the wafer level. You presently fabricate your circuits on wafers with a usable area of 3 square inches. The cost of processing a single wafer is $40, and yields are such that you currently sell your amplifier for one dollar. Your chief engineer describes a new amplifier that he has designed. It has characteristics far superior to your present model and can be made by the same process, but it requires a chip size of 0.05 inch by 0.1 inch. Explain to your engineer the effect this change would have on selling price. You may assume that wafer defects are randomly distributed.

P10.2

A current repeater of the type shown in Fig. 10.9 is investigated with a transistor curve tracer. The ground connection in this figure is connected to the curve-tracer emitter terminal, the input is connected to the base terminal of the tracer, and the repeater output is connected to the collector terminal of the curve tracer. Assume that both transistors have identical values for I_S and very high current gain. Draw the type of a display you expect on the curve tracer.

P10.3

Assume that it is possible to fabricate lateral-PNP transistors with a current gain of 100 and a value of C_π equal to 400 pF at 100 μA of collector current. A unity-gain current repeater is constructed by bisecting the collector of one of these transistors and connecting the device as shown in Fig. 10.10. Calculate the 0.707 frequency of the current transfer function for this structure operating at a total collector current of 100 μA. You may neglect C_μ and base resistance for the transistor. Contrast this value with the frequency at which the current gain of a single-collector lateral-PNP transistor with similar parameters drops to 0.707 of its low-frequency value.

P10.4

Figure 10.26 shows a connection that can be used as a very low level current source. Assume that all transistors have identical values of I_S, high β, and are at a temperature of 300° K. Find values for R_1, R_2, and R_3 such that the output current will be 1 μA subject to the constraint that the sum of the resistor values is less than 100 kΩ.

P10.5

Consider the three current repeater structures shown in Figs. 10.9, 10.11*a*, and 10.11*b*. Assume perfectly matched transistors, and calculate the

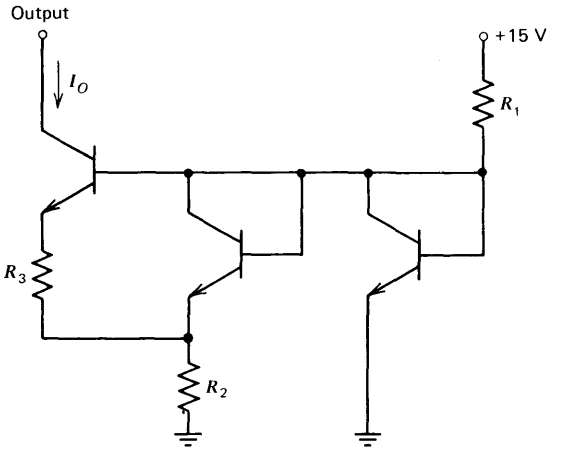


Figure 10.26 Very low level current source.

incremental output resistance of each connection in terms of β and η of the transistors and the operating current level.

P10.6

The final voltage-gain stage and output buffer of an integrated-circuit operational amplifier is shown in Fig. 10.27. Calculate the quiescent collector-current level of the complementary emitter follower. You may assume that the current gain of the NPN transistors is 100, while that of PNP's is 10. You may further assume that all NPN's have identical characteristics, as do all PNP's.

P10.7

An operational amplifier input stage is shown in Fig. 10.28. Calculate the drift referred to the input of this amplifier attributable to changes in current gain of the transistors used in the current repeater. You may assume that these transistors are perfectly matched, have a common-emitter current gain of 100, and a fractional change in current gain of 0.5% per degree Centigrade. Suggest a circuit modification that reduces this drift.

P10.8

A portion of the biasing circuitry of the LM101A operational amplifier is shown in Fig. 10.29. This circuit has the interesting property that for a properly choosen operating current level, the bias voltage is relatively insensitive to changes in the current level. Determine the value of I_B that makes $\partial V_O/\partial I_B$ zero. You may assume high current gain for both transistors.

P10.9

Determine how unity-gain frequency and slew rate are related to the first-stage bias current for the μA776 operational amplifier. Use the specifi-

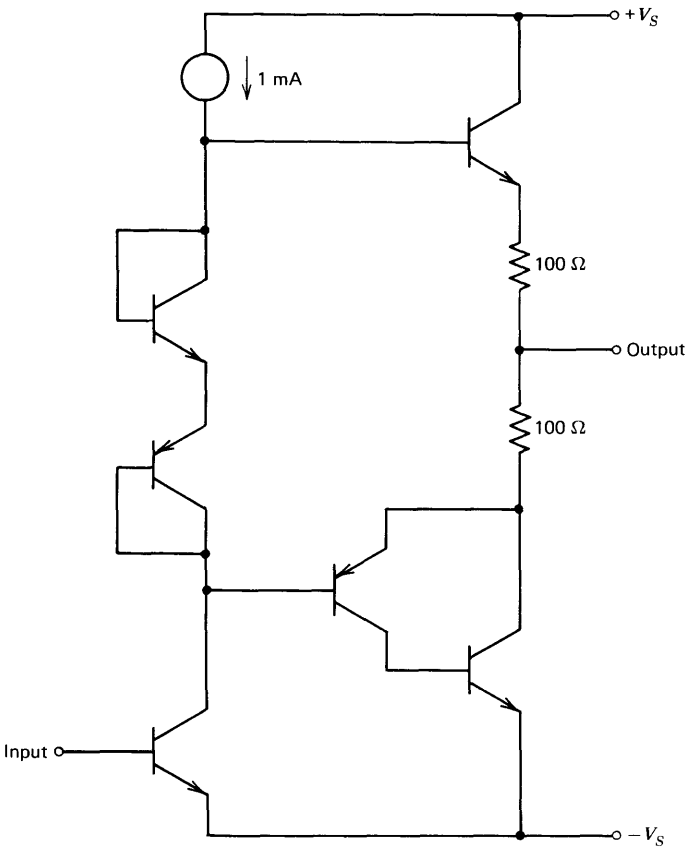


Figure 10.27 Amplifier output stage.

cations for this amplifier to estimate input-stage quiescent current at a set-current value of 1.5 μA. Assuming that the ratio of bias current to set current remains constant for lower values of set current, estimate the 10 to 90% rise time in response to a step for the μA776 connected as a non-inverting gain-of-ten amplifier at a set current of 1 nA. Also estimate slew rate and power consumption for the μA776 at this set current.

P10.10

A μA776 is connected in a loop with a LM101A as shown in Fig. 10.30.

(a) Show that this is one way to implement a function generator similar to that described in Section 6.3.3.

(b) Plot the transfer characteristics of the LM101A with feedback (i.e., the voltage v_A as a function of v_B).

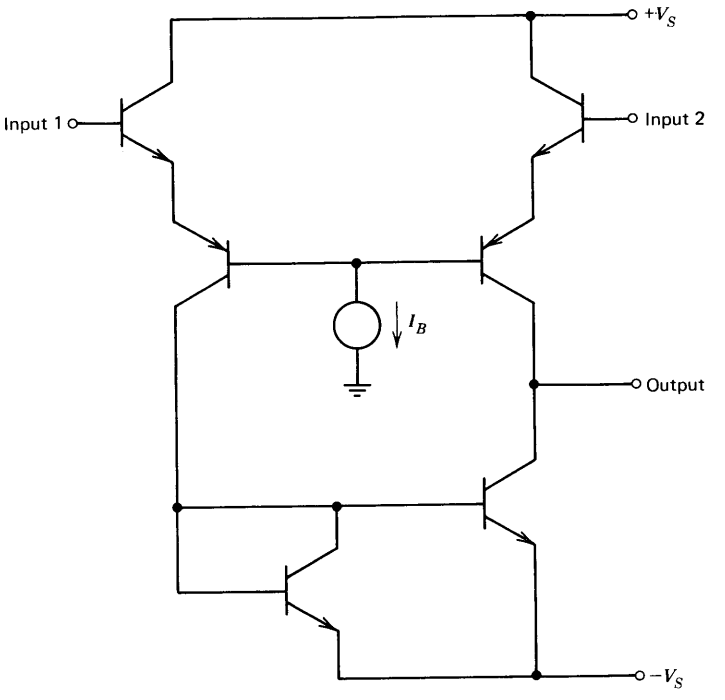


Figure 10.28 Amplifier input stage.

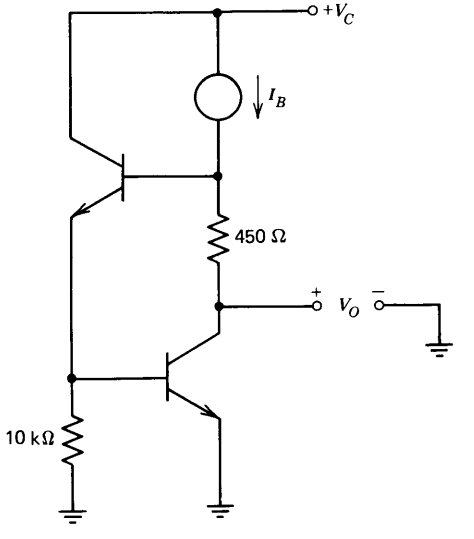


Figure 10.29 Bias circuit.

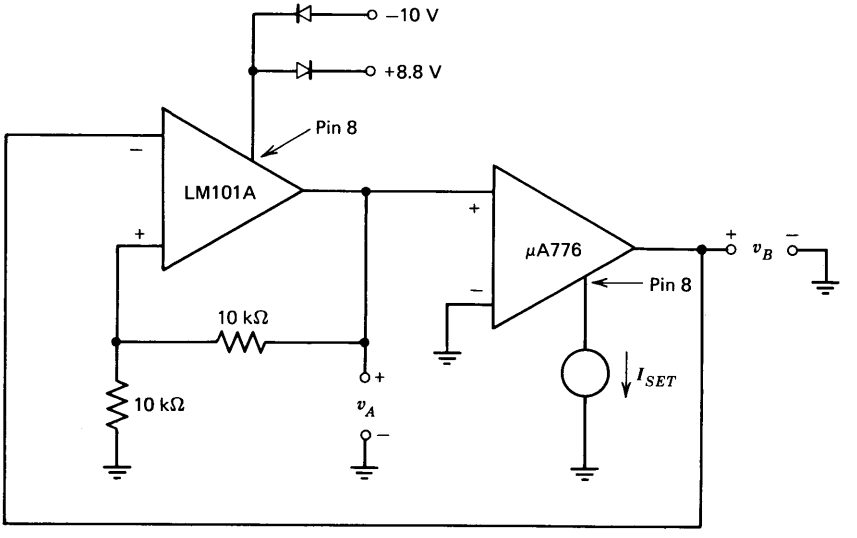


Figure 10.30 Nonlinear oscillator.

(c) Draw the waveforms $v_A(t)$ and $v_B(t)$ for this circuit. You may assume that the slew rate of the 101A is much greater than that of the μA776.
(d) How do these waveforms change as a function of I_{SET}?

P10.11

A simplified schematic of an operational amplifier is shown in Fig. 10.31.

(a) How many stages has this amplifier?
(b) Make the (probably unwarranted) assumption that all transistors have identical (high) values for β and identical values for η. Further assume that appropriate pairs have matched values of I_S. Calculate the low-frequency gain of the amplifier.
(c) Calculate the amplifier unity-gain frequency and slew rate as a function of the current I, the capacitor C_c, and any other quantities you need. You may assume that this capacitor dominates amplifier dynamics.
(d) Suggest a circuit modification that retains essential features of the amplifier performance, yet increases its low-frequency voltage gain.

P10.12

Specifications for the LM101A operational amplifier indicate a maximum input bias current of 100 nA and a maximum temperature coefficient of input offset current (input offset current is the difference between the bias current required at the two amplifier inputs) of 0.2 nA per degree Centigrade. These specifications apply over a temperature range of −55° C to +125° C. Our objective is to precede this amplifier with a matched pair of 2N5963

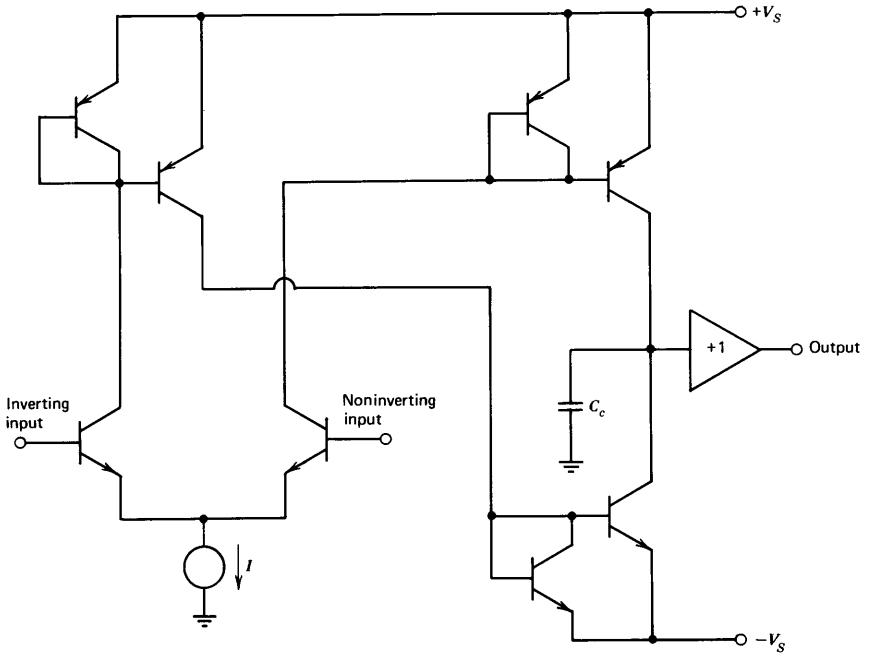


Figure 10.31 Operational amplifier.

transistors connected as emitter followers so that it can be used in applications that require very low input currents. Assume that you are able to match pairs of 2N5963 transistors so that the difference in base-to-emitter voltages of the pair is less than 2 mV at equal collector currents. Design an emitter-follower circuit using one of these pairs and any required bias-circuit components with the following characteristics:

1. The bias current required at the input of the emitter followers is relatively independent of common-mode level over the range of ± 10 volts.
2. The drift referred to the input added to the complete circuit by the emitter followers is less than ± 2 μV per degree Centigrade. Indicate how you plan to balance the emitter-follower pair in conjunction with the amplifier to achieve this result.

Estimate the input current for the modified amplifier with your circuit, assuming that the common-emitter current gain of the 2N5963 is 1000. Estimate the differential input resistance of the modified amplifier. You will probably need to know the differential input resistance of the LM101A to complete this calculation. In order to determine this quantity, show that for the LM101A input-stage topology, differential input resistance can be determined from input bias current *alone*.

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