CHAPTER IX

AN ILLUSTRATIVE DESIGN

9.1 CIRCUIT DESCRIPTION

The purpose of this section is to illustrate by example one way that the basic two-stage amplifier can be expanded into a complete, useful operational amplifier. Later sections of this chapter analyze the circuit to determine its performance, show how it can be compensated in order to tailor its open-loop transfer function for use in specific applications, and indicate how design alternatives might affect performance.

No attempt is made to justify this particular implementation of the two-stage amplifier other than to point out that the circuit was designed at least in part for its educational value. An appreciation of the salient features of this particular circuit leads directly to improved understanding of other operational amplifiers, including a number of integrated-circuit designs, which have evolved from the basic topology. The modifications incorporated into the basic design are certainly not the only possible ones, nor are they all likely to be required in any given application. The circuit does illustrate how a designer might resolve some of the tradeoffs available to him, and also provides a background for much of the material in later sections.

9.1.1 Overview

The complete circuit and important quiescent levels are shown in Fig. 9.1. The circuit represents a modification of the basic amplifier that combines a differential amplifier incorporating several of the drift minimizing techniques described in Chapter 7 with a high-gain stage consisting of a current-source-loaded cascode amplifier. A unity-voltage-gain buffer amplifier isolates the high-resistance node at the output of the cascode amplifier and provides high current output drive capability. The amplifier is designed to provide a ± 10-volt maximum output signal and operate from standard ± 15-volt supplies. The supply voltages are both bypassed with a parallel combination of an electrolytic and a ceramic capacitor, since this combination is effective over a wide frequency range.

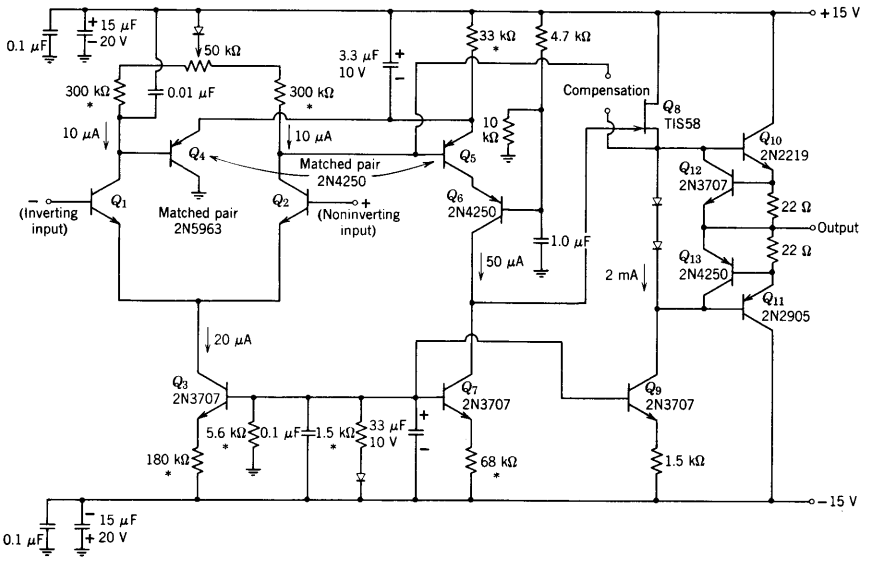


Figure 9.1 Discrete-component operational amplifier. *Note.* *Indicates 1% metal-film resistor.

This circuit shares a characteristic with a number of other moderately involved designs, which is often disturbing to novice circuit designers since there is some difficulty in determining which transistors are actually in the signal path. It is important to resolve this uncertainty prior to any detailed discussion of the circuit. Referring to Fig. 9.1, we see that transistors Q_1 and Q_2 are the differential-amplifier input stage. As we shall see, the second-stage topology constrains the emitter connection of the Q_4-Q_5 pair to be incrementally grounded. Thus Q_5 and Q_6 form a cascode amplifier. This current-source-loaded cascode provides the largest fraction of the amplifier gain, with analysis to be presented indicating a voltage gain of 180,000 in this portion of the circuit.

The high-resistance node at the output of the cascode amplifier is isolated with source-follower-connected FET Q_8. The source follower drives transistors Q_{10} and Q_{11}, which are connected as a complementary emitter follower.

The amplifier can be compensated by connecting an appropriate network between the indicated terminals, thereby forming a minor loop that includes the high-gain stage. Details of this process are given in Section 9.2.3.

The above discussion shows that the signal path includes only transistors Q_1, Q_2, Q_5, Q_6, Q_8, Q_{10}, and Q_{11}. The remaining transistors are used either

as current sources (Q_3, Q_7, and Q_9), or to reduce voltage drift referred to the input by forming a differential second stage at d-c (Q_4), or to limit output current (Q_{12} and Q_{13}).

9.1.2 Detailed Considerations

Once the topology of the circuit is selected, a decision concerning approximate bias-current levels is a necessary first step in the detailed design process. Low current levels give improved d-c performance since input currents and input-stage self-heating are reduced. However, the frequency response of the amplifier is reduced by operation at low currents. (See Section 9.3.3 for a description of power-speed tradeoffs.)

A compromise collector current level of 10 μA, which can provide excellent d-c performance combined with closed-loop frequency response of several MHz, was selected for the first-stage transistors. Transistor Q_3 is a current source that provides the total 20-μA quiescent current of the first stage and insures high common-mode rejection ratio. This current source shares a common bias network with two other current sources. The bias network includes a diode that provides approximate temperature compensation for the current sources, and also includes capacitive bypassing to the negative supply. Bypassing to the negative supply rather than to ground is preferable in this case since it insures that the current-source output is independent of high-speed transients on the negative supply line.

The differential input stage is a matched pair of 2N5963 transistors. The devices are selected to have base-to-emitter voltages matched to within 3 mV at equal collector currents and, furthermore, to have current gains matched to within 10% at the operating current level. They are mounted in close thermal proximity to reduce temperature differentials. Wrapping wire around the pair or mounting them in an aluminum block drilled to accept the transistors improves the thermal bond. The 2N5963 is selected because it is inexpensive and provides a typical current gain of 1100 at a collector current of 10 μA. The resultant bias current required at either input is approximately 10 nA without any form of current compensation. Compensating techniques such as these described in Section 7.4.2 can be used to lower this bias current to less than 1 nA over a 50° C temperature range.

Transistors Q_5 and Q_6 are the cascode-amplifier transistors. An additional PNP transistor, Q_4, is used to improve d-c performance by forming a differential amplifier with transistor Q_5. While this transistor lowers drift, it does not affect the operation of the Q_5-Q_6 pair in any way as shown by the following discussion. It is evident that at low frequencies the common-emitter point of pair Q_4-Q_5 is incrementally grounded since only differential signals

can be applied to this pair by the input stage. The capacitor[1] included across the 33-kΩ emitter-circuit resistor guarantees that the emitter of Q_5 also remains incrementally grounded at high frequencies. Since transistor Q_4 is included only to improve d-c performance and is not required for gain at any frequency, its base circuit can be bypassed at moderate and high frequencies. Bypassing insures that Q_1 operates as a common-collector stage at these frequencies. It was mentioned in the last chapter that operation in this mode is advantageous since it minimizes the input capacitance seen at the base of Q_1 (the inverting input of the complete amplifier), and thus allows a wider range of feedback networks to be used without significant high-frequency loading.

The amplifier is balanced by changing relative collector load resistor values in the first stage. Since the input-stage transistors are matched for a maximum base-to-emitter voltage differential of 3 mV at equal collector currents, the ratio of the collector currents will be at most $e^{3mV(q/kT)} \simeq 1.12$ at equal base-to-emitter voltages. The 50-kΩ potentiometer that allows a maximum collector-resistor ratio of 1.17:1 is therefore adequate for balancing even if some mismatch of second-stage base currents exists. The diode included in the Q_1-Q_2 collector circuit provides a degree of compensation for the base-to-emitter voltage changes of transistors Q_4-Q_5 with temperature in order to stabilize their quiescent current.

The 2N4250 transistors used in the second stage are one of the highest-gain PNP types available, with a typical current gain in excess of 300 at 50 μA of collector current. This gain permits a five-to-one increase in quiescent operating level between the first and second stages (valuable since this increase improves the bandwidth of the second-stage devices) without seriously compromising drift performance. It also contributes to high overall amplifier gain. While it is not necessary to use the same transistor type for both members of a cascode amplifier pair, the 2N4250 is also used in the common-base section of the cascode (Q_6) since it has high r_μ, a necessary condition for high voltage gain. The 2N3707 used as the current-source load for the cascode is also selected in part because of high r_μ.

All critical resistors associated with the first two stages are precision metal film types. These are preferred since their low temperature coefficients reduce voltage drift and because of their low noise characteristics.

A field-effect transistor is used to isolate the high-impedance node at the cascode output. The virtually infinite input resistance of the FET improves

[1] As a matter of practical interest, eliminating this capacitor has only a minor effect on the overall performance of the amplifier, but complicates the analysis. This is an example of a component included primarily for educational purposes.

voltage gain. Component economy is also achieved, since an additional stage of current gain would probably be required for isolation if bipolar transistors were used. A current source is used for FET bias so that the bias current is independent of output-voltage level. The quiescent level of this stage is chosen to meet maximum drive requirements for the following stage.

A complementary emitter-follower pair (Q_{10}-Q_{11}) is used to provide large positive or negative output currents with minimum quiescent power dissipation. Metal-can rather than epoxy-cased transistors are used in this stage for increased power-handling capability. The two diodes included in the base circuit of the emitter-follower pair reduce crossover distortion, while the 22-Ω resistors eliminate the possibility of thermal runaway that accompanies this connection.

Transistors Q_{12} and Q_{13} combine with the 22-Ω resistors to limit the output current of the amplifier to approximately 30 mA. This limiter circuit, which is similar in operation to the diode limiter described in connection with Fig. 8.27, is used since it is identical in form to one frequently used in integrated-circuit designs. Consider the limiting process when the amplifier output voltage is negative. If the sink current exceeds 25 to 30 mA, transistor Q_{13} conducts, since its base-to-emitter voltage approximates 600 mV. This conduction reduces base drive for Q_{11}. The current that must be conducted by Q_{13} in order to eliminate base drive to Q_{11} is at most 2 mA, the output level of current source Q_9.

When the amplifier output voltage is positive, transistor Q_{12} conducts to limit output current. This situation is potentially hazardous, since it is conceivable that the driving transistor (Q_8) could be destroyed if no mechanism limited its drain current. However, the geometry of the TIS58 is such that its drain current is the order of 5 mA when the gate-to-source voltage of this device reaches the forward-conduction value. Thus, while transistor Q_{12} may conduct approximately 3 mA in positive output current limit, destruction of Q_8 is not possible. Note also that since the maximum collector current of Q_6 is limited to modest values by the 33-kΩ emitter-circuit resistor associated with Q_4-Q_5, the maximum current from Q_6 cannot injure any devices.

No attempt is made to control internal amplifier voltages, such as the emitter potential of Q_5, during current overload. The charge stored on the 3.3-μF capacitor delays recovery from overload, but since current limit is not anticipated during normal operation (overload protection is included primarily to protect us from our own errors during system breadboarding), this delay is unimportant.

9.2 ANALYSIS

In order to demonstrate the performance features of the amplifier introduced in the previous section, it is necessary to approximate analytically some of its more important characteristics. While the exact details of the analysis are specific to this amplifier, several significant features, particularly those concerning dynamics and compensation, are common to all two-stage operational amplifiers. Thus the conclusions we shall reach extend beyond this particular circuit.

We should realize that certain aspects of the following analysis are likely to be in error by a factor of two or more, since the uncertainty of some of the parameter values associated with the transistors limits accuracy. Another type of difficulty is encountered in the analysis of the dynamics of the amplifier, since a number of poles are predicted in the vicinity of the f_T of the transistors used in the amplifier. Such results are always suspect because transistor-model deficiencies prevent accurate analysis in this frequency range. Fortunately, these inaccuracies are of little concern since our objective is not so much precise prediction of the performance of this particular amplifier as it is an understanding of the important features of this general type of amplifier.

9.2.1 Low-Frequency Gain

One important characteristic of an operational amplifier is its d-c open-loop gain. Calculation of the gain of this amplifier is necessary because accurate measurement of the signal levels that would permit experimental gain determination is precluded by noise and drift.

By far the largest fraction of the low-frequency gain of the amplifier occurs in the cascode stage for this particular implementation of the basic topology. The analysis of the complete amplifier is facilitated by initially developing a low-frequency equivalent circuit for the cascode amplifier. The analysis of Section 8.3.4 showed that the voltage gain of an unloaded cascode amplifier is

$$-\frac{\beta_6}{2\eta_6} = -\frac{g_{m6}r_{\mu 6}}{2}$$

while its input resistance is $r_{\pi 5}$. (Subscripts differentiating between the two transistors in the cascode connection refer to Fig. 9.1.) While the output resistance of the cascode connection was not specifically calculated, a result from Section 8.3.5 can be used to determine this quantity. Equation 8.59 gives $r_\mu/2$ as the output resistance of a common-base current source with a large incremental emitter-circuit resistance. The output resistance of the cascode must be identical since its output consists of a common-base

connection with a large emitter-circuit resistance. These results show that the low-frequency performance of the cascode portion of the amplifier can be modeled by the equivalent circuit of Fig. 9.2.

The d-c gain of the circuit shown in Fig. 9.1 is determined using the parameter values shown in Table 9.1 for the transistors. The calculation is performed assuming that the noninverting input of the amplifier is incrementally grounded. This assumption yields the same value for d-c gain that would be obtained considering a true differential input voltage. Incrementally grounding the noninverting input does eliminate an insignificant high-frequency term in the transfer function that results from signals fed through the collector-to-base capacitance of Q_2 (see Section 8.2.3).

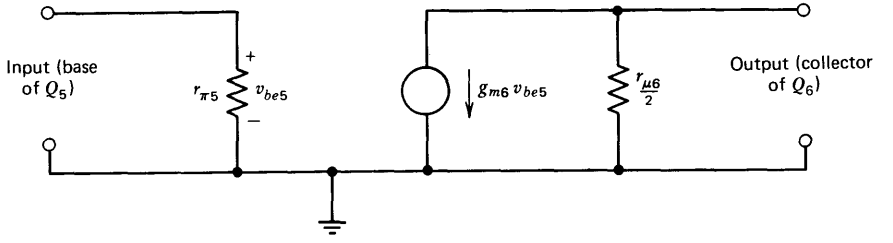


Figure 9.2 Equivalent circuit for cascode amplifier at low frequencies.

Table 9.1 Transistor Parameters for Circuit of Fig. 9.1

Transistor Number	Type	I_C or I_D (μA)	g_m (mmho)	β	r_π (kΩ)	r_μ (MΩ)	r_o (MΩ)	C_μ or C_{gd} (pF)	C_π or C_{gs} (pF)
Q_1, Q_2	2N5963	10	0.4	1100	2750	*	*	6	10
Q_3	2N3707	20	*	*	*	*	*	8	10
Q_4, Q_5, Q_6	2N4250	50	2	350	175	500	1.4	10	15
Q_7	2N3707	50	2	200	100	500	2.5	8	10
Q_8	TIS58	2 mA	*	—	—	—	—	2	*
Q_9	2N3707	2 mA	*	*	*	*	*	*	*
Q_{10}	2N2219	*	*	200	*	*	*	*	*
Q_{11}	2N2905	*	*	200	*	*	*	*	*
Q_{12}	2N3707	0	*	*	*	*	*	*	*
Q_{13}	2N4250	0	*	*	*	*	*	*	*

— Not relevant.

* Value unimportant in included analysis.

Overall gain is found by first calculating the transfer relationships for various portions of the circuit. An incremental input voltage applied to the base of Q_1, v_i, causes a change in the collector current of Q_2 given by

$$i_{c2} = -\frac{v_i g_{m1}}{2} \tag{9.1}$$

(It has been assumed that both input transistors are operating at equal currents so that $g_{m1} = g_{m2}$.)

The previously developed cascode equivalent circuit shows that the change in base voltage of Q_5 is related to the Q_2 collector-current change by

$$v_{be5} = -i_{c2}(325\ \text{k}\Omega \| r_{\pi 5}) \tag{9.2}$$

(The collector-circuit potentiometer has been assumed set to center position so that the load resistor of transistor Q_2 is equal to 325 kΩ.) In order to determine the voltage gain of the cascode amplifier, it is necessary to calculate the load applied to it. The input resistance of field-effect transistor Q_8 is essentially infinite, while the output resistance for the current source Q_7 is

$$r_{\mu 7} \left\| \left[\frac{1 + g_{m7}(r_{\pi 7} \| 68\ \text{k}\Omega)}{g_{o7}} \right] \right. \tag{9.3}$$

(See Eqn. 8.57.) It is computationally convenient to reduce this equation now and to introduce the experimentally verifiable assumption that $r_{\mu 7} \simeq r_{\mu 6}$. This value is reasonable, since both devices are operating at identical currents, and are fabricated using similar (though complementary) processing. The 2N3707 has a typical β of 200 at 50 μA, so that $r_{\pi 7}$ is typically 100 kΩ at this current. Therefore, $r_{\pi 7} \| 68\ \text{k}\Omega \simeq 0.4 r_{\pi 7}$. Accordingly, the output resistance of Q_7 becomes

$$r_{\mu 7} \left\| \left[\frac{1 + g_{m7}(0.4 r_{\pi 7})}{g_{o7}} \right] \right. \simeq r_{\mu 7} \left\| \left[\frac{0.4\beta_7}{g_{o7}} \right] \right. = r_{\mu 7} \| 0.4 r_{\mu 7} \simeq 0.28 r_{\mu 7} \tag{9.4}$$

Using this relationship, the assumed equivalence of $r_{\mu 7}$ and $r_{\mu 6}$, and the model of Fig. 9.2 shows that the loaded cascode voltage gain is

$$\frac{v_{cb6}}{v_{be5}} \simeq -g_{m6}\left(\frac{r_{\mu 6}}{2} \| 0.28 r_{\mu 6}\right) \simeq -g_{m6}(0.18 r_{\mu 6}) \tag{9.5}$$

Recognizing that the unloaded voltage gain from the collector of Q_6 to the amplifier output is unity and combining Eqns. 9.1, 9.2, and 9.5 yields

$$\frac{v_o}{v_i} = -\frac{g_{m1}}{2}(325\ \text{k}\Omega \| r_{\pi 5}) g_{m6}(0.18 r_{\mu 6}) \tag{9.6}$$

Substituting parameter values from Table 9.1 into Eqn. 9.6 predicts a d-c open-loop gain magnitude of 4×10^6. The gain is dominated by the contribution of 1.8×10^5 from the cascode amplifier (see Eqn. 9.5).

9.2.2 Transfer Function

The locations of all poles and zeros of the amplifier could be predicted for the complete circuit by substituting appropriate incremental models for the active devices, although this would be a formidable task even with the aid of a computer. The approach used here is to make relatively crude approximations to gain insight into the controlling dynamics of the amplifier and then to verify the approximate results with a more detailed (though still incomplete) computer analysis.

The unloaded low-frequency voltage gain of the buffer amplifier (transistors Q_8 through Q_{11}) is unity. Amplifier loads as low as several hundred ohms do not appreciably alter its performance. If the load applied to the amplifier is not capacitive, the frequency response of the buffer approaches the f_T of the devices used in it. Furthermore, the input impedance of Q_8, which loads the cascode amplifier, is independent of any load applied to the amplifier output since the FET is unilateral. Thus the influence of the buffer can be modeled by simply using the input capacitance of Q_8, C_{gd8}, as a load for the cascode. Similarly, the loading of transistor Q_7 can be represented as a parallel impedance consisting of its output capacitance $C_{\mu 7}$ and output resistance $0.28r_{\mu 7}$ (Eqn. 9.4).

An incremental model that reflects these simplifications is shown in Fig. 9.3. The base resistances (r_x's) of all transistors, as well as r_μ and r_o of transistors other than Q_6 and Q_7 (the transistors in the high-gain portion of the circuit) have also been ignored. An argument based on the concept of open-circuit time constants[2] is used to further simplify this model. The open-circuit resistances[3] facing capacitors $C_{\pi 1}$, $C_{\mu 1}$, $C_{\pi 2}$, $C_{\mu 3}$, and $C_{\pi 6}$ are all on the order of $1/g_m$ for the related transistor or lower. Thus these capacitors do not affect the dynamics of the amplifier at frequencies low compared to the f_T's of the various transistors and are eliminated for the initial approximation. As a result of this approximation the only contribution of the input stage to amplifier dynamics is a consequence of the loading $C_{\mu 2}$ applies to the base of Q_5, and the stage itself can be modeled as a single dependent current source.

[2] See P. E. Gray and C. L. Searle, *Electronic Principles: Physics, Models, and Circuits*, Wiley, New York, 1969, Chapters 15 and 16.

[3] The open-circuit resistance facing a capacitor is the incremental resistance at the terminal pair in question calculated with all other capacitors in the circuit removed or open-circuited.

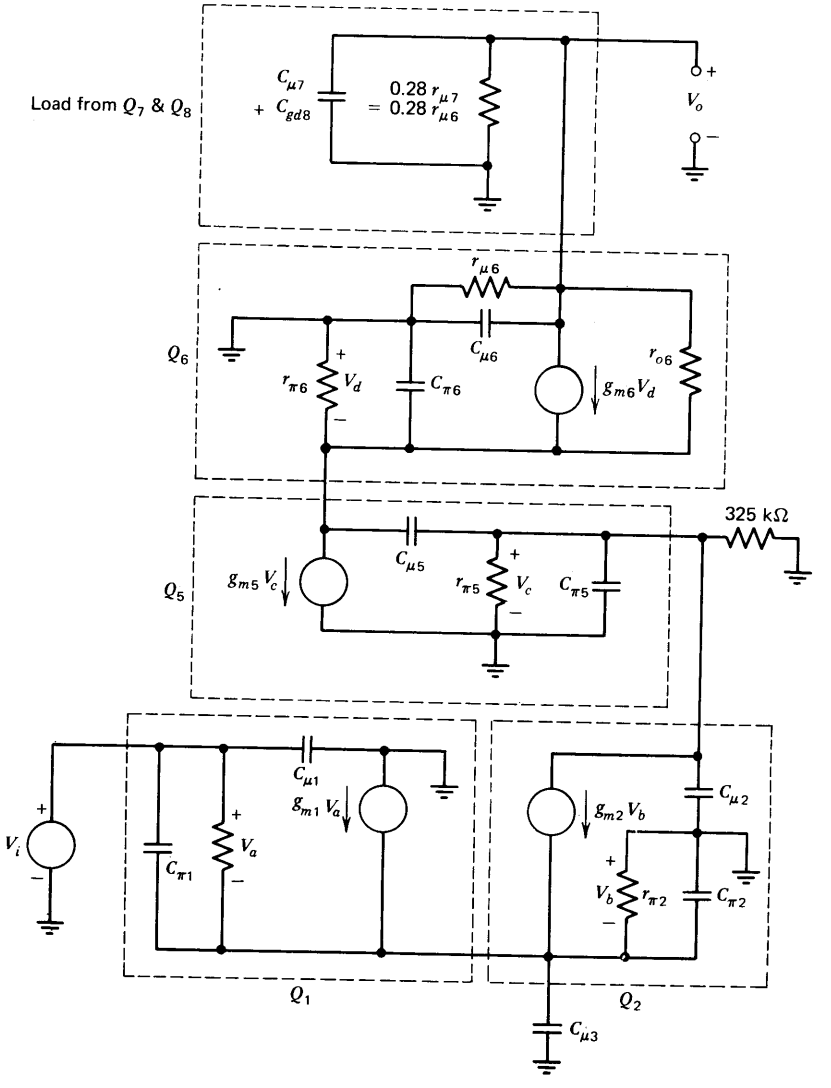


Figure 9.3 Model used to determine transfer function.

The further-simplified incremental model incorporating the approximations introduced above and shown in Fig. 9.4 is used to approximate the location of the two low-frequency amplifier poles. The node equations for this circuit are

$$\frac{g_{m1}V_i}{2} = [(C_1 + C_{\mu 5})s + G_1]V_a - C_{\mu 5}sV_b$$

$$0 = (-C_{\mu 5}s + g_{m5})V_a + (C_{\mu 5}s + g_{m6} + g_{\pi 6} + g_{o6})V_b - g_{o6}V_o$$

$$0 = (-g_{m6} - g_{o6})V_b + (C_2 s + g_{o6} + G_2)V_o \qquad (9.7)$$

(See Fig. 9.4 for the definition of parameters in this equation.)

The poles are found by equating the determinant of the matrix of coefficients of Eqn. 9.7 to zero, yielding

$$\frac{C_1 C_2 C_{\mu 5}}{g_{m6}G_1(G_2 + g_{\mu 6})}s^3 + \frac{C_2(C_1 + 2C_{\mu 5})}{G_1(G_2 + g_{\mu 6})}s^2 + \frac{C_2}{G_2 + g_{\mu 6}}s + 1 = 0 \qquad (9.8)$$

In reducing Eqn. 9.7 to 9.8, small terms have been dropped. However, *only* terms that are small because of transistor and topological inequalities such as $g_m \gg g_\pi \gg g_o \gg g_\mu$, and $C_2 > C_{\mu 6}$ since one component of C_2 is $C_{\mu 6}$ have been eliminated. Thus the conclusions that will be drawn from Eqn. 9.8 are applicable to a variety of circuits that share this topology

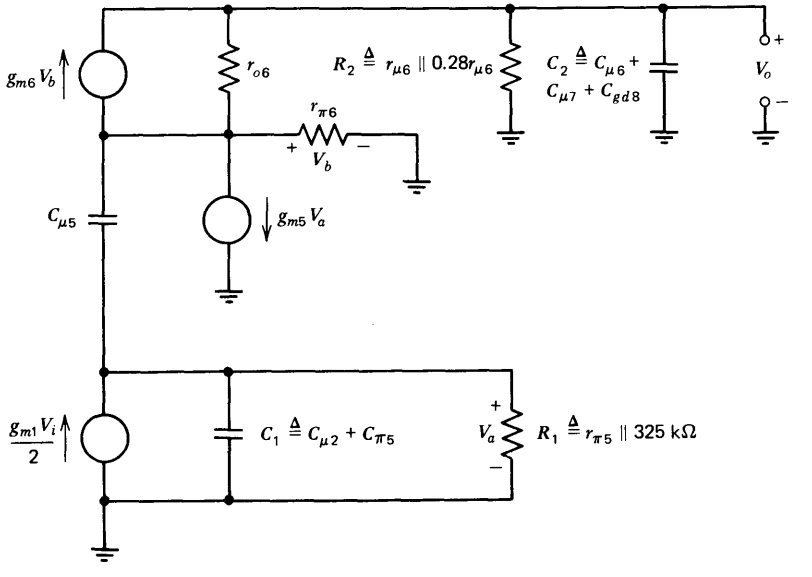


Figure 9.4 Simplification of Fig. 9.3.

rather than being limited to the specific choice of element values shown in Fig. 9.1. Fundamental relationships among parameter values also insure that the three poles represented by Eqn. 9.8 will be real and widely spaced. Consequently, this cubic equation can be easily factored, since

$$(\tau_a s + 1)(\tau_b s + 1)(\tau_c s + 1) \simeq \tau_a\tau_b\tau_c s^3 + \tau_a\tau_b s^2 + \tau_a s + 1$$

$$\text{for} \quad \tau_a \gg \tau_b \gg \tau_c \tag{9.9}$$

Equation 9.9 allows us to write Eqn. 9.8 as

$$\left(\frac{C_2}{G_2 + g_{\mu 6}} s + 1\right)\left(\frac{C_1 + 2C_{\mu 5}}{G_1} s + 1\right)\left(\frac{C_1 C_{\mu 5}}{g_{m6}(C_1 + 2C_{\mu 5})} s + 1\right) = 0 \tag{9.10}$$

indicating that

$$\begin{aligned} \tau_a &= \frac{C_2}{G_2 + g_{\mu 6}} \\ \tau_b &= \frac{C_1 + 2C_{\mu 5}}{G_1} \\ \tau_c &= \frac{C_1 C_{\mu 5}}{g_{m6}(C_1 + 2C_{\mu 5})} \end{aligned} \tag{9.11}$$

The physical interpretation of the time constants lends insight into the operation of the circuit. The resistance associated with time constant τ_a is simply the incremental resistance from the high resistance node (the collector of Q_6) to ground. [Recall that $1/(G_2 + g_{\mu 6}) = 0.28r_{\mu 6} \parallel r_{\mu 6} \parallel r_{\mu 6} = 0.18r_{\mu 6}$, the value obtained earlier and used in Eqn. 9.5 for the incremental resistance from this node to ground.] Similarly, capacitance $C_2 = C_{\mu 6} + C_{\mu 7} + C_{gd8}$ is the capacitance from the high resistance node to ground. Since the capacitance of all amplifier nodes is the same order of magnitude, it is not surprising that the dominant amplifier pole is associated with energy storage at the highest resistance node. Substituting values from Table 9.1 shows that $\tau_a = 1.8$ ms, implying that the dominant amplifier open-loop pole is located at $s = -550$ sec^{-1}.

Time constant τ_b is associated with the resistance and capacitance from the base of Q_5 to ground. The conductance G_1 in Eqn. 9.11 was defined previously as the conductance from this node to ground. The capacitance consists of the collector-to-base capacitance of Q_2 that shunts this node and the total effective input capacitance (including that attributed to Miller effect) Q_5 would display if this transistor were loaded with a resistive load equal to $1/g_{m5}$. Note that at frequencies much above $1/\tau_a$ radians per second, the capacitive loading at the collector of Q_6 has reduced the voltage

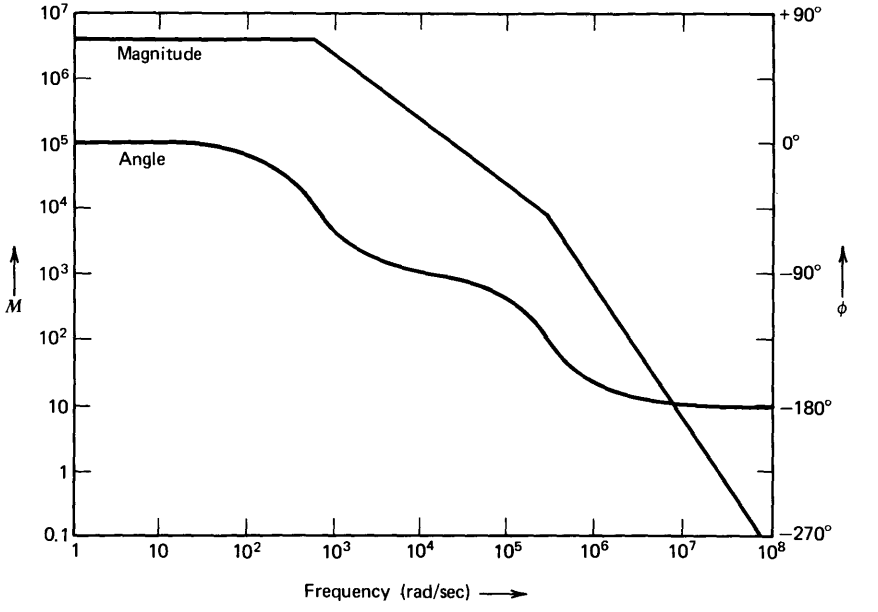


Figure 9.5 Amplifier open-loop transfer function based on two lowest-frequency poles (no compensation).

gain of this transistor; as a result, there is no significant feedback to the emitter of Q_6 through r_{o6} at these frequencies. Thus transistor Q_6 provides the $1/g_{m6} = 1/g_{m5}$ load for Q_5. The time constant τ_b is equal to 4.5 μs, implying that the second amplifier pole is located at $s = -2.2 \times 10^5$ sec^{-1}. Time constant τ_c corresponds to a frequency that approximates f_T for the transistors in the circuit, and thus to one of many high-frequency poles that are ignored in the simplified analysis.

Combining the d-c gain (Eqn. 9.6) with the dynamics predicted above yields

$$\frac{V_o(s)}{V_i(s)} = \frac{-4 \times 10^6}{(1.8 \times 10^{-3}s + 1)(4.5 \times 10^{-6}s + 1)} \tag{9.12}$$

Equation 9.12 is shown as a Bode plot[4] in Fig. 9.5.

[4] The transfer function plotted in Fig. 9.5 is actually the negative of Eqn. 9.12. This modification is made because we anticipate using the amplifier in negative-feedback connections. Since the loop transmission has the same sign as the gain calculated for the amplifier in these applications, plotting the negative of the amplifier gain follows the convention of plotting the negative of the loop transmission of a feedback system. Viewed alternatively, the transfer function plotted in Fig. 9.5 would result if the input signal were applied to the noninverting input terminal of the amplifier.

The pole locations for this design were also predicted by computer analysis, in order to verify some of the assumptions introduced in the preceding development. The equivalent circuit of Fig. 9.3 with 100-Ω base resistors added to the circuit model for each transistor was analyzed. Thus only the buffer amplifier was eliminated from the computer calculations. The locations of the two dominant poles predicted by the computer were -520 sec^{-1} and -2.15×10^5 sec^{-1}. All other poles had break frequencies in excess of 10^7 radians per second. In spite of the seemingly drastic approximations included in the analysis of this circuit, the predicted locations of the two dominant poles are confirmed by the computer calculation to within round-off errors.

9.2.3 A Method for Compensation

The transfer function of this amplifier (Eqn. 9.12) has the poles separated by a factor of 400, and in many feedback amplifiers this amount of separation would seem ideal from a stability point of view. Unfortunately, with the massive low-frequency open-loop gain characteristic of operational amplifiers (4×10^6 in this design), greater separation is required to insure adequate stability in many applications. For example, if the amplifier is used as a unity-gain follower by connecting its output to its inverting input, a loop is formed with $a(j\omega)$ as shown in Fig. 9.5 and $f = 1$. The Bode plot shows that the phase margin of the system is approximately 0.5° in this case, clearly an unsatisfactory value. In practice, this configuration would be unstable, since the negative phase shift associated with neglected open-loop singularities is far greater than 0.5° at the amplifier unity-gain frequency. It is clear that some method must be used to modify the open-loop transfer function of the amplifier in order to achieve acceptable performance in this and many other connections.

One of the significant advantages of the amplifier configuration described in this section and of all amplifiers that share its topology is that it is possible to use internal feedback to provide easily predicted and well-controlled compensation. The compensation is implemented by connecting a network between the terminals marked compensation in Fig. 9.1. This network completes a minor loop that includes the high-gain stage. Since both dominant amplifier poles are included inside the local feedback loop, it is possible to alter the location of the most important poles in the amplifier transfer function by this type of internal feedback. The degree of control that minor-loop feedback can exercise on the transfer function of a two-stage amplifier was hinted at in Section 5.3 and in the discussion of the effects of C_μ of the high-gain stage in Section 8.2.3.

There are at least two important limitations to this type of compensation. First, since this compensation is a form of negative feedback, the magnitude of the compensated open-loop amplifier transfer function will be less than or equal to the magnitude of the uncompensated transfer function at most frequencies. While resonances introduced by the minor feedback loop may give a gain increase at one or two particular frequencies, the bandwidth over which such increases exist is necessarily limited. Second, there is some maximum frequency for which this is an effective method of compensation, since beyond this frequency the influence of other singularities, some of which are outside the compensating loop and therefore cannot be controlled, become important. While these singularities are all at frequencies comparable to the f_T's of the transistors, they do set the ultimate bandwidth limitation of the amplifier because of the phase shift that they contribute to its open-loop transfer function at frequencies of interest. For example, at 1/10 of its break frequency, a 10th-order pole contributes 57° of negative phase shift to a transfer function but only changes the magnitude by 5%. In practice, the unity-gain frequency of the amplifier-feedback network combination is normally chosen to limit the phase contribution of the high-frequency singularities to less than 30° at this frequency so that stability is not compromised. It is often necessary to determine the frequency at which the phase shift of higher-order singularities becomes important experimentally because of the difficulties associated with accurate analytic prediction of their locations.

An incremental model for the amplifier of Fig. 9.1 that can be used to analyze the effects of the internal feedback used for compensation is shown in Fig. 9.6. The development of this model relies heavily on the analysis of Section 9.2.2. The input impedance of the amplifier, which is unimportant for purposes of this calculation, is Z_i. An input voltage forces a proportional current at the node including the base of Q_5.[5]

The impedance at the base of Q_5 is modeled as a parallel R-C network with a time constant equal to τ_b in Eqn. 9.11. The remainder of the cascode is modeled as an impedance equal to the impedance from the collector of Q_6 to ground driven by a dependent-current source supplying a current $g_{m6}V_{be5}$. The impedance transformation of the field-effect transistor is represented as a unity-voltage-gain buffer amplifier. The complementary emit-

[5] This representation assumed an input voltage applied to the inverting input of the amplifier. If voltages are applied to both inputs, the differential voltage is used for V_i. An advantage of this type of amplifier is that the dynamics of the first stage do not significantly influence the transfer function at frequencies of interest; thus it functions as a true differential-input amplifier.

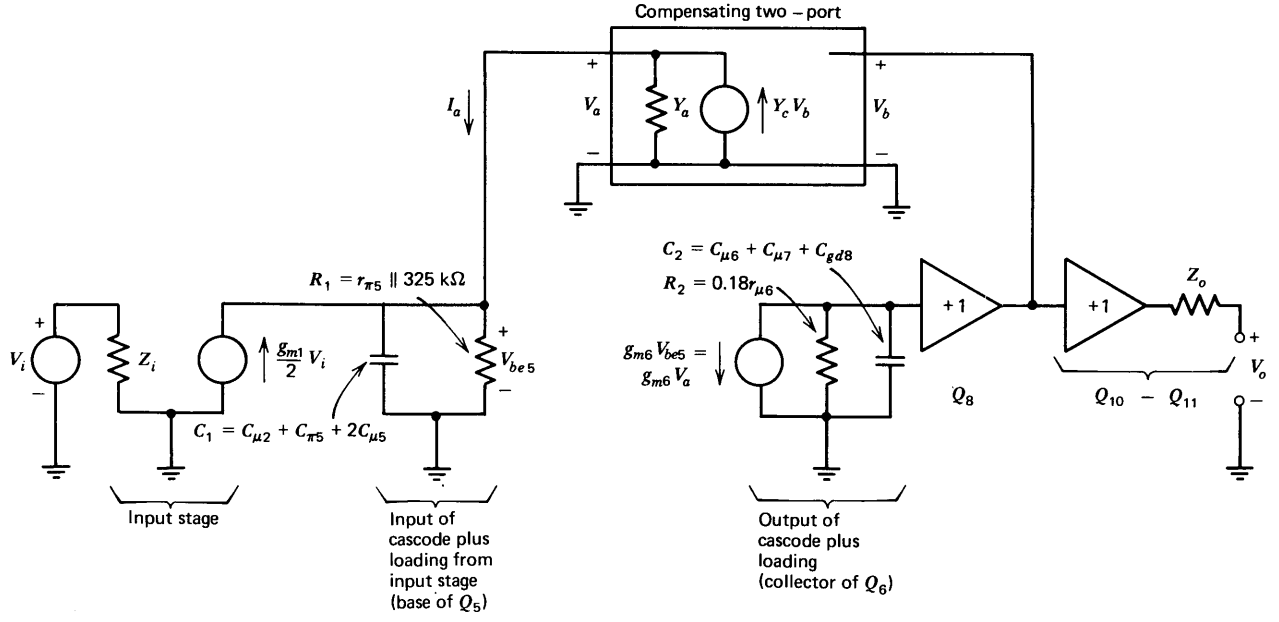


Figure 9.6 Model used to illustrate method of compensation.

ter-follower pair is modeled as a second buffer amplifier with an output impedance Z_o.

The compensating minor loop is formed by connecting a two-port network between the output of the source follower and the base of Q_5. Since the right-hand port of the network is driven by the low-impedance source follower, the voltage V_b is independent of V_a; thus the two-port can be completely represented in this application by the two admittances[6]

$$Y_a = -\frac{I_a}{V_a} \qquad V_b = 0 \tag{9.13a}$$

$$Y_c = \frac{I_a}{V_b} \qquad V_a = 0 \tag{9.13b}$$

Node equations for the model of Fig. 9.6 are

$$\frac{g_{m1}}{2} V_i = (Y_1 + Y_a)V_a - Y_c V_b \tag{9.14}$$

$$0 = g_{m6} V_a + Y_2 V_b$$

where

$$Y_1 = \frac{1}{R_1} + C_1 s$$

$$Y_2 = \frac{1}{R_2} + C_2 s$$

Recognizing that output voltage V_o is identical to V_b in the absence of load allows us to determine the gain of the amplifier from Eqn. 9.14 as

$$\frac{V_o}{V_i} = \frac{V_b}{V_i} = -\frac{(g_{m1}/2)g_{m6}/[(Y_1 + Y_a)Y_2]}{1 + g_{m6}Y_c/[(Y_1 + Y_a)Y_2]} \tag{9.15}$$

The quantity $g_{m6}Y_c/[(Y_1 + Y_a)Y_2]$ is identified as the negative of the loop transmission of the inner loop formed when the amplifier is compensated. In many cases of practical interest, the phase angle of this expression is close to plus or minus 90° when its magnitude is unity. The 90° phase margin of the compensating loop then insures that there is no peaking in its response. In these cases a very simple approximation serves to determine the magnitude of the open-loop transfer function of the amplifier, and the

[6] These definitions differ from those conventionally used to describe two-port networks in that the reference direction for I_a is out of the network. This choice reduces the number of minus signs in the following equations.

approximation yields a result that is correct within a factor of 0.707 at all frequencies. The implication from 9.15 is that

$$\frac{V_o(j\omega)}{V_i(j\omega)} \simeq -\frac{g_{m1}}{2Y_c(j\omega)} \tag{9.16}$$

at frequencies where

$$\left| \frac{g_{m6}Y_c(j\omega)}{[Y_1(j\omega) + Y_a(j\omega)]Y_2(j\omega)} \right| > 1$$

and

$$\frac{V_o(j\omega)}{V_i(j\omega)} \simeq -\frac{g_{m1}}{2} \frac{g_{m6}}{[Y_1(j\omega) + Y_a(j\omega)]Y_2(j\omega)} \tag{9.17}$$

at all other frequencies. Thus, when the minor-loop transmission magnitude is large, the open-loop transfer function of the amplifier is controlled by the minor-loop feedback element.

This approximation is particularly easy to apply graphically. The open-loop transfer function of the amplifier without compensation, but with the compensating network loading the base of Q_5, is plotted on log-magnitude vs. log-frequency coordinates. The proper loading is realized by connecting one side of the network to the base of Q_5 in the usual manner, and by disconnecting the other side of the network from the source of Q_8 and connecting it instead to an incremental ground. This first plot is particularly easy to obtain if a single capacitor is used as the compensating element (the most frequent case because this compensation leads to an approximately single pole open-loop transfer function) since only the location of the higher-frequency pole in Eqn. 9.12 is changed. The magnitude of the expression $g_{m1}/2Y_c(j\omega)$ is also plotted on the same coordinates. The magnitude of the amplifier open-loop transfer function at any frequency is then approximately equal to the lower magnitude of the two plotted curves. This relationship is easily developed from Eqns. 9.16 and 9.17, by noticing that the gain of the amplifier with the shorted compensating network connected to the base of Q_5 is

$$\frac{g_{m1}}{2} \frac{g_{m6}}{(Y_1 + Y_a)Y_2}$$

and that if

$$\left| \frac{g_{m1}}{2Y_c} \right| < \left| \frac{g_{m1}}{2} \frac{g_{m6}}{(Y_1 + Y_a)Y_2} \right|$$

then

$$\left| \frac{g_{m6}Y_c}{(Y_1 + Y_a)Y_2} \right| > 1$$

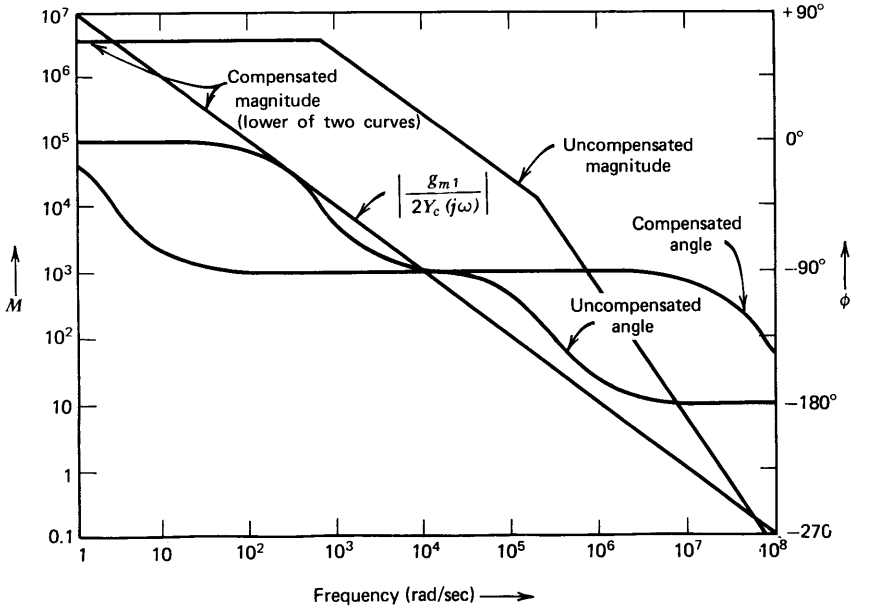


Figure 9.7 Effect of compensation.

Figure 9.7 illustrates the effects of compensating the amplifier shown in Fig. 9.1 with a 20-pF capacitor. The quantities Y_c and Y_a for this compensating network are both equal to $2 \times 10^{-11}s$. One of the two curves is obtained directly from the uncompensated transfer function of Fig. 9.5 by moving the second pole from 2.2×10^5 radians per second to 1.5×10^5 radians per second, since loading by the compensating capacitor increases the total capacitance at the base of Q_5 by 50%. The second plot is

$$\left|\frac{g_{m1}}{2Y_c(j\omega)}\right| = \frac{10^7}{\omega}$$

The curve for the compensated amplifier is the lower of the two plots at all frequencies.

The advantages of this compensation for certain applications are obvious. It was shown earlier that operation with $f = 1$ would cause the uncompensated amplifier to oscillate. If a 20-pF compensating capacitor is used, the phase margin of the amplifier with direct feedback is greater than 45°.

Note that this compensation lowers the first amplifier open-loop pole to 2.5 radians per second. The location of the low-frequency pole cannot be independently chosen if we insist on a single-pole rolloff at frequencies

below the unity-gain frequency and constrain both the unity-gain frequency and the d-c gain. The pole must be located at a frequency equal to the ratio of the unity-gain frequency to the d-c gain. This pole does not compromise closed-loop bandwidth, since closed-loop bandwidth is determined by the crossover frequency of the loop.

It is worth mentioning that parameter values for this amplifier are such that the uncompensated open-loop transfer function will be noticeably modified by any capacitive compensation in excess of approximately 0.1 pF! The minimum capacitor value necessary to modify the amplifier transfer function can be determined by noting that the uncompensated magnitude curve shown in Fig. 9.5 includes a region where its value is $2 \times 10^9/\omega$. Thus, if a capacitor in excess of 0.1 pF is used for compensation, the magnitude $|g_{m1}/2Y_c(j\omega)|$ will be smaller than the uncompensated magnitude over some frequency range. Furthermore, it is evident that feedback from any high level part of the circuit (from the collector of Q_6 on) back to the base circuit of Q_5 has approximately the same effect as feedback via the compensation terminals. Inevitable stray capacitance between these two parts of the circuit is usually on the order of 1 pF, and it is therefore concluded that the "uncompensated" curve of Fig. 9.7 can probably never be measured for an actual amplifier.

As indicated above, feedback from any portion of the circuit from the collector of Q_6 on modifies performance in much the same way as feedback from the source of Q_8, and in certain applications it may be advantageous to compensate by feeding back from an alternate point. For example, feedback from the output terminal includes more of the amplifier inside the compensating loop and thus with the control of this loop. Unfortunately, compensating-loop stability is less certain for this type of minor-loop feedback. Similarly, if large capacitors are used for compensation, greater inner-loop stability may be achieved by compensating from the collector Q_6.

Some of the reasons for selecting an amplifier topology with the possibility for this type of compensation should now be clear. The compensation is normally chosen so that it, rather than uncompensated amplifier dynamics, dominates amplifier performance at all frequencies of interest. Thus the open-loop transfer function of the amplifier with compensation becomes quite reliable. A wide variety of open-loop transfer functions can be obtained (several examples will be given in Chapter 13) with the main limitation being the requirement of maintaining the stability of the compensating loop. Furthermore, it is easy to determine what compensating network should be used to produce a given open-loop transfer function.

9.3 OTHER CONSIDERATIONS

A myriad of performance characteristics combine to determine the overall utility of an operational amplifier. The possibilities for modifications that compromise one characteristic in order to enhance another are numerous in this type of complex circuit. While the major advantage of the two-stage design centers on its easily controlled dynamics, the topology can be readily tailored to specific applications by other types of modifications. This section indicates a few of the "hidden" features of the two-stage design and points out the possibility of certain types of design compromises.

9.3.1 Temperature Stability

The last section shows that the use of internal feedback to compensate the amplifier under discussion yields an open-loop transfer function inversely proportional to the transfer admittance of the compensating network over a wide range of frequencies. The constant of proportionality for this and other variations of the two-stage design includes the transconductance of either input transistor, and is thus inversely related to temperature if the collector current of these transistors is temperature independent. This relatively mild variation with temperature is tolerable in many applications.

If greater transfer-function stability is required, the input-stage bias current can be made directly proportional to the absolute temperature. As a result, input-stage transconductance, and therefore the open-loop transfer function, will be temperature independent. A further advantage of this type of bias-current variation is that it partially compensates for input-transistor current-gain variations with temperature and thus reduces input-current changes.

The required bias-current temperature dependence can be implemented by appropriate selection of the total voltage applied to the base-to-emitter junction and the emitter resistor of the input-stage current source (Q_3 in Fig. 9.1). It can be shown that the output current from the source will be directly proportional to temperature if this voltage is constant and is approximately equal to the energy-band-gap voltage V_{go} (see Problem P9.11).

9.3.2 Large-Signal Performance

The analysis of the effects of compensation on amplifier performance has been limited up to now to linear-region operation. It is clear that compensation also effects large-signal behavior. For example, an open-loop transfer function similar to that obtained using a 20-pF compensating capacitor could be obtained by connecting a series-connected 3.6-μF capacitor and 500-Ω resistor from the base of Q_5 to ground. However, recovery from over-

load might be greatly delayed with this type of compensation because of the time required to change the voltage on a 3.6-μF capacitor with the limited current available at this node.

The compensation also limits the *slew rate*, or maximum time rate of change of output voltage of the amplifier. Consider an output voltage time rate of change $\dot{v}_O$. If a compensating capacitor C_c is used, the capacitor current required at the node including the base of Q_5 is $C_c\dot{v}_O$. The maximum magnitude of the current that can be supplied to this node by the first stage and that is available to charge the capacitor is approximately equal to the quiescent bias current of either input transistor I_{C1}. Thus the slew rate is $\dot{v}_O(\text{max}) = I_{C1}/C_c$. However, the ratio I_{C1}/C_c also controls the unity-gain frequency of the amplifier, since this frequency is $g_{m1}/2C_c = qI_{C1}/2kTC_c$. The important point is that if some consideration, such as the phase shift from high-frequency singularities, limits the unity-gain frequency, it also limits the slew rate if a single capacitor is used to compensate the amplifier.

One way to circumvent this relationship is to add equal-value emitter resistors to both input transistors so that the transconductance of the input stage is lower than $g_{m1}/2$. Unfortunately, emitter degeneration also degrades the drift of the amplifier. Another more attractive possibility is the use of more involved compensation than that provided by a single capacitor. This alternative will be discussed in Chapter 13.

9.3.3 Design Compromises

There are many variations of the basic amplifier topology that result in useful designs, and some of these variations will be illustrated in Chapter 10. Other degrees of freedom are possible by varying quiescent operating current and by changing transistor types. The purpose of this section is to indicate how these variations influence amplifier performance.

Consider the changes that result from increasing all quiescent operating currents by a factor K. This change can be effected by decreasing all circuit resistors by the same factor. In response to the current change, all internal transistor resistances will decrease by the same factor, since all are multiples of $1/g_m$. Current gains of the various transistors do not change significantly if K is not grossly different from one. Thus the d-c voltage gain, which is a ratio of transistor and circuit conductances of the amplifier, will not change in response to changes in quiescent current. Input current will increase directly with quiescent current, and drift may increase somewhat because of increased self-heating in the first stage.

The dynamics for the design in question (at least without compensation) are determined primarily by the resistance and capacitance values at the base of Q_5 and at the collector of Q_6. The resistance values at these nodes

decrease by an amount K, since they consist of combinations of transistor and circuit resistances. The capacitance values remain constant, at least for moderate changes from the levels used in the last sections, for the following reason. The capacitances involved are transistor-junction capacitances C_{gd}, C_{μ}, and C_{π}. Capacitances C_{gd} and C_{μ} are current-level independent, while C_{π} is the sum of a constant term plus a component linearly proportional to current. For transistor types likely to be used in this circuit, the current-proportional term is not important at levels below 1 mA. Thus an increase in current levels by as much as a factor of 10 from the values indicated in Fig. 9.1 does not significantly change critical node capacitances.

The argument above shows that moderate increases in operating current cause proportional increases in the locations of uncompensated open-loop poles. The form of the amplifier uncompensated open-loop transfer function remains unchanged and is simply shifted toward higher frequency. The possibility for increased bandwidth after compensation as a result of this modification is evident.

A second alternative is to change the relative ratios of first- and second-stage currents. An increase in second-stage current relative to that of the first stage has three major effects:

1. Drift increases because second-stage loading becomes more significant.
2. Gain decreases because the input resistance of the second stage decreases.
3. Bandwidth increases because the second-stage resistances decrease.

Significant flexibility is afforded by the choice of the active devices. The transistor types shown in Fig. 9.1 were selected primarily for high values of β and $1/\eta$. These types result in an amplifier design with high d-c voltage gain, low input current, and low drift. Unfortunately, because of compromises necessary in transistor fabrication, these types may have relatively high junction capacitances.

Clearly higher-frequency transistors can be used in the design. In fact, amplifiers with this topology have been operated with closed-loop bandwidths in excess of 100 MHz by appropriately selecting transistor types and operating currents. However, the d-c voltage gain for a design using high-frequency transistors is usually one to two orders of magnitude lower than that of the design shown in Fig. 9.1. Input current and voltage drift are also severely degraded. Furthermore, many high-frequency transistors have breakdown voltages on the order of 10 to 15 volts, resulting in limited dynamic range for an amplifier using such transistors.

At times high-frequency types are used for transistors Q_4 and Q_5, with high-gain types used in other locations. This change improves the band-

width of the amplifier, but compromises voltage gain and drift because of the lower current gain typical of high-frequency transistors. Since transistors Q_4 and Q_5 operate at low voltage levels, dynamic range is not altered.

9.4 EXPERIMENTAL RESULTS

While the amplifier described in this chapter was designed primarily as an educational vehicle, it has been built and tested, and can be used to demonstrate certain performance features of the two-stage design. Although a detailed description of the experimentally measured performance of this amplifier is of questionable value since it is not a commercially available

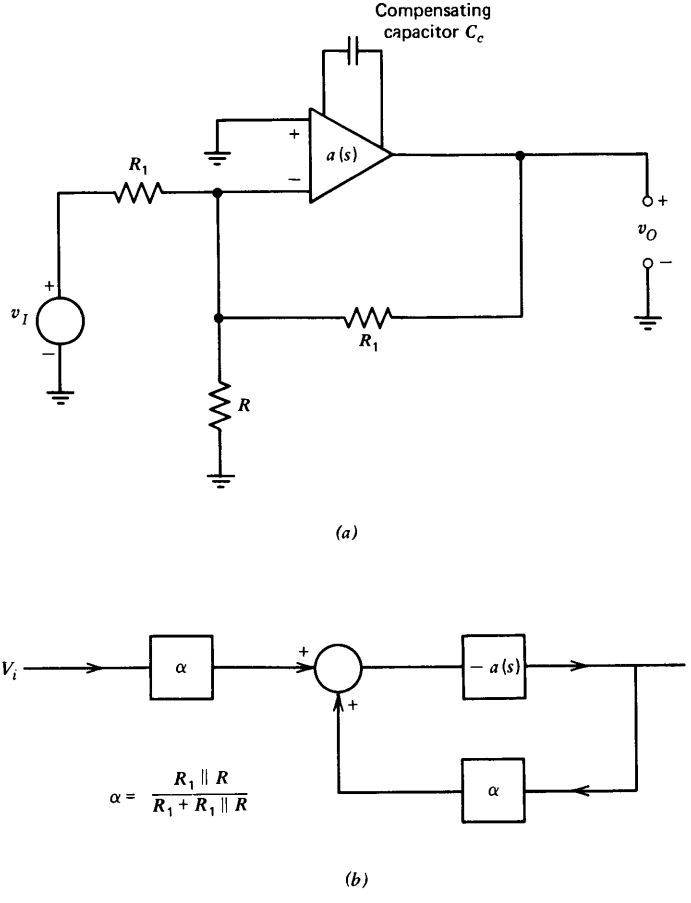


Figure 9.8 Inverting amplifier. (*a*) Circuit. (*b*) Block diagram.

design, the presentation of several transient responses seems a worthwhile prelude to the more detailed experimental evaluation of compensation included in Chapter 13.

The amplifier was connected as shown in Fig. 9.8*a*. This connection, which results in the block diagram shown in Fig. 9.8*b*, is useful for demonstrations since it permits control of the loop transmission both by selection of the value of C_c [which influences $a(s)$] and by choice of R. The ideal closed-loop gain of the connection is minus one independent of R.

The magnitude of the loop transmission for this system, with only the lowest-frequency pole included, is shown in Bode-plot form in Fig. 9.9. As anticipated, the crossover frequency is dependent on the ratio α/C_c.

The output of the amplifier in response to -20-mV step input signals with $R = \infty$ ($\alpha = 1/2$) for four different values of compensating capacitor is shown in Fig. 9.10. Note that for the larger values of C_c, the response is very nearly first order, and that the 10 to 90% rise time agrees closely with the value predicted for single-pole systems, $t_r = 2.2/\omega_c$. Smaller compensating-capacitor values change the character of the response as the system becomes relatively less stable and faster. The highly oscillatory response that results for $C_c = 5$ pF indicates that the phase shift added at the crossover frequency by the second- and higher-frequency poles is very nearly 90° in this case.

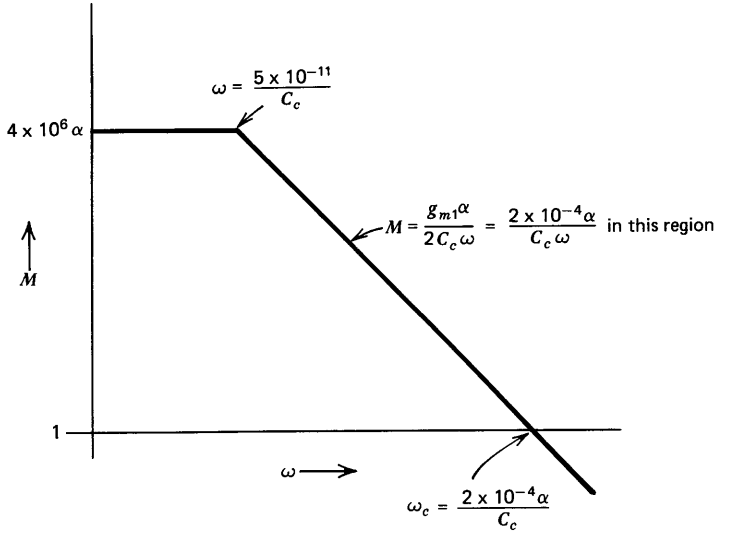


Figure 9.9 Loop-transmission magnitude for inverting amplifier.

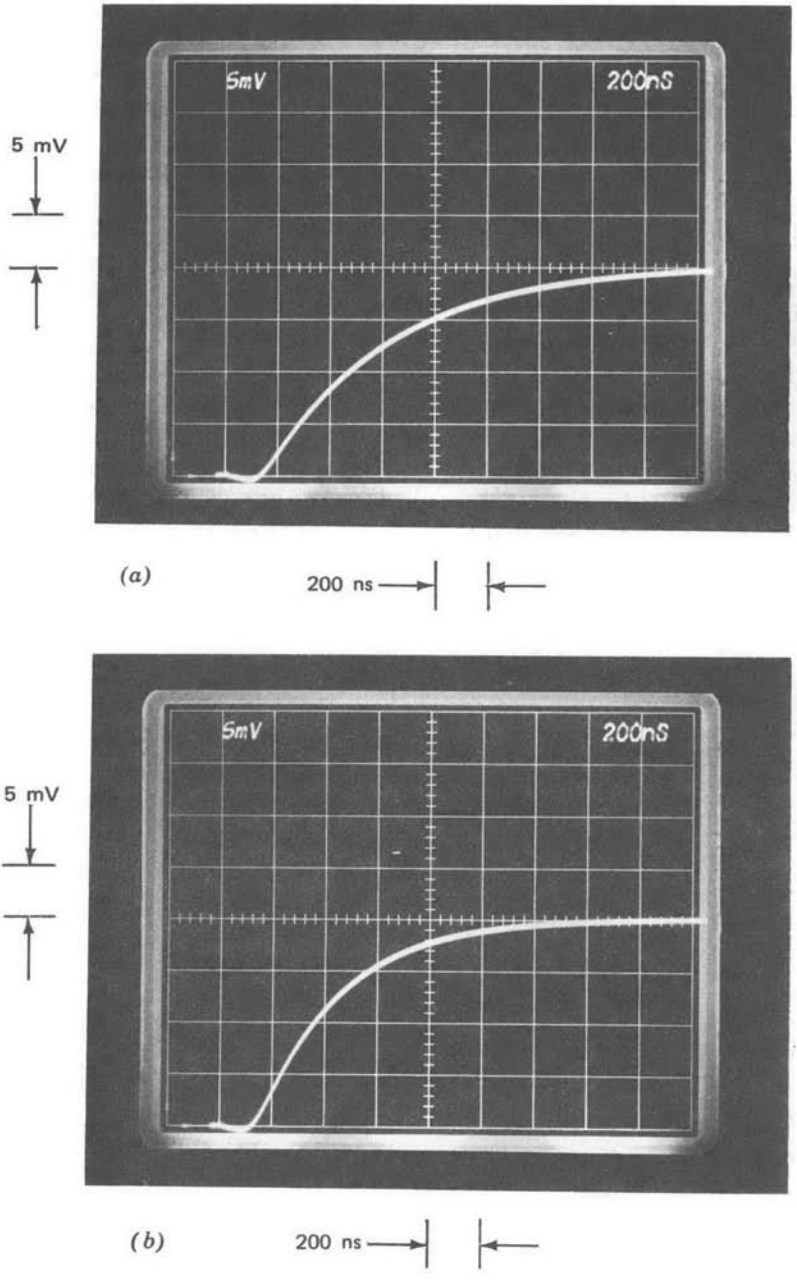
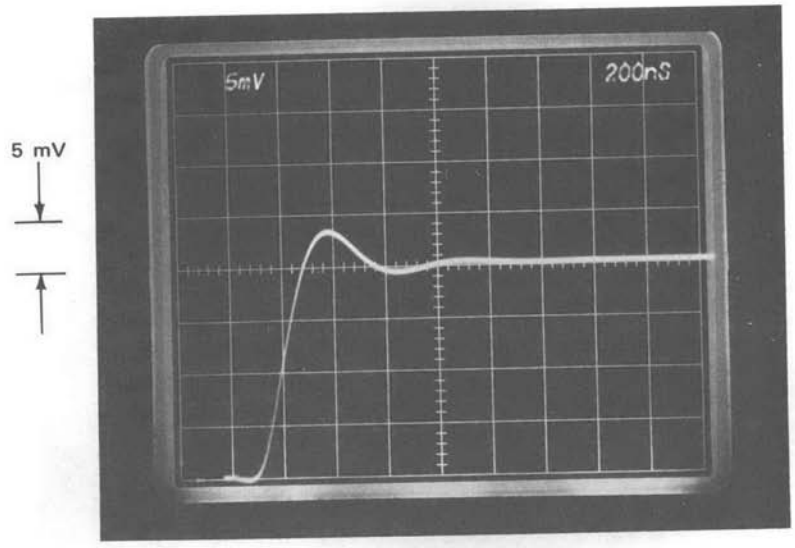
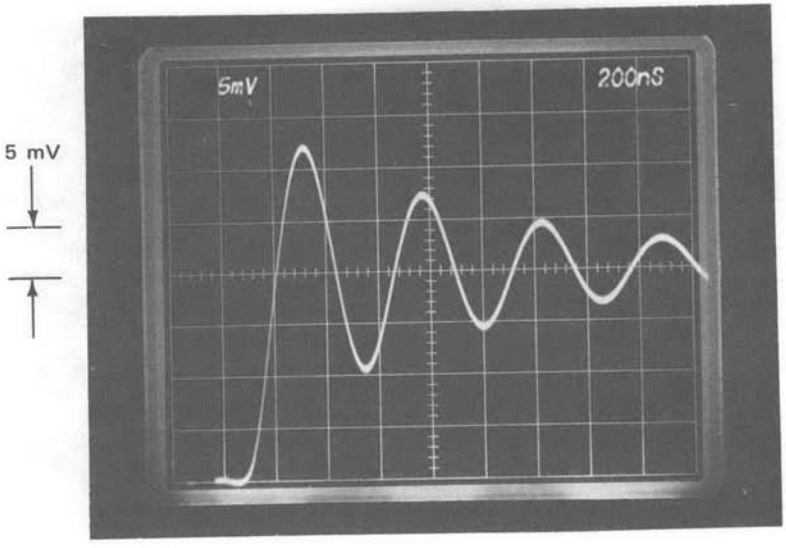


Figure 9.10 Closed-loop step response as a function of compensating capacitor (input-step amplitude is −20 mV). (*a*) $C_c = 47$ pF. (*b*) $C_c = 33$ pF. (*c*) $C_c = 10$ pF. (*d*) $C_c = 5$ pF.



(c) 200 ns



(d) 200 ns

Figure 9.10—Continued

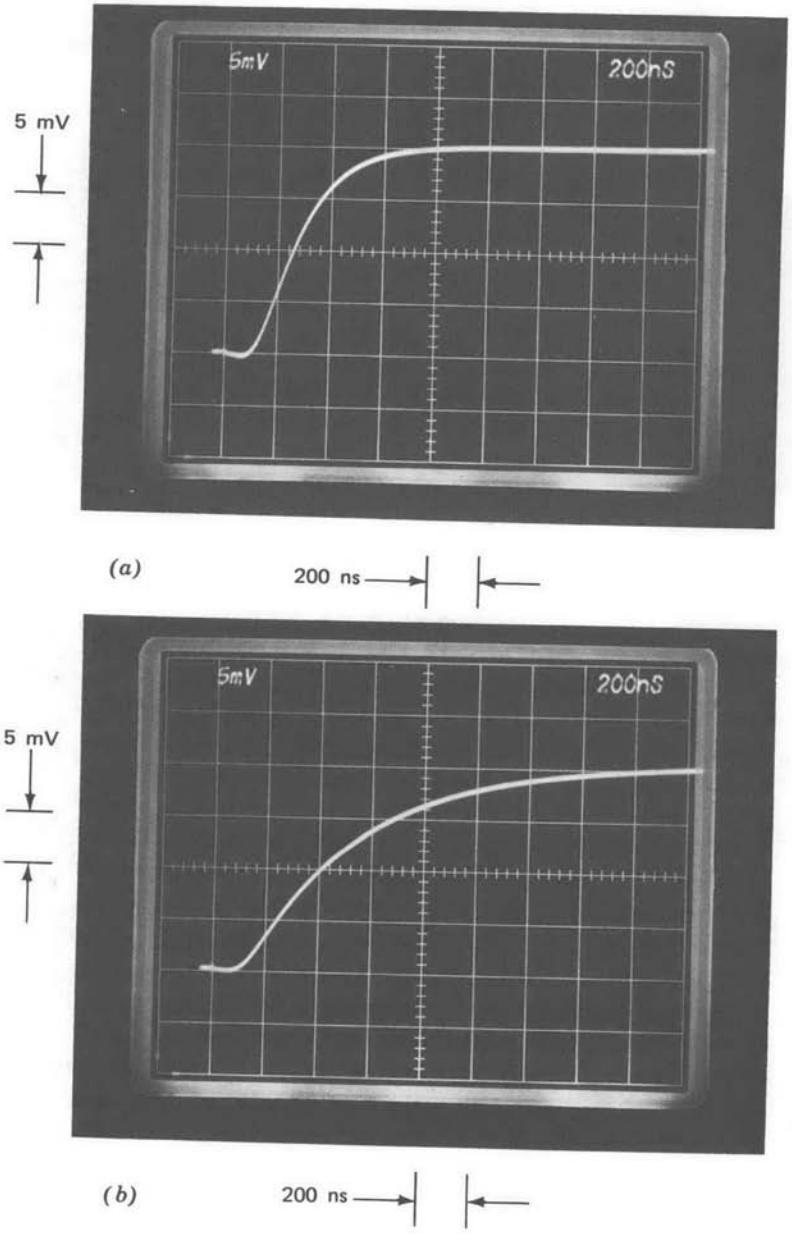


Figure 9.11 Step response as a function of compensating capacitor and α (input-step amplitude is -20 mV). (*a*) $C_c = 20$ pF, $\alpha = 1/2$. (*b*) $C_c = 20$ pF, $\alpha = 1/4$. (*c*) $C_c = 10$ pF, $\alpha = 1/4$.

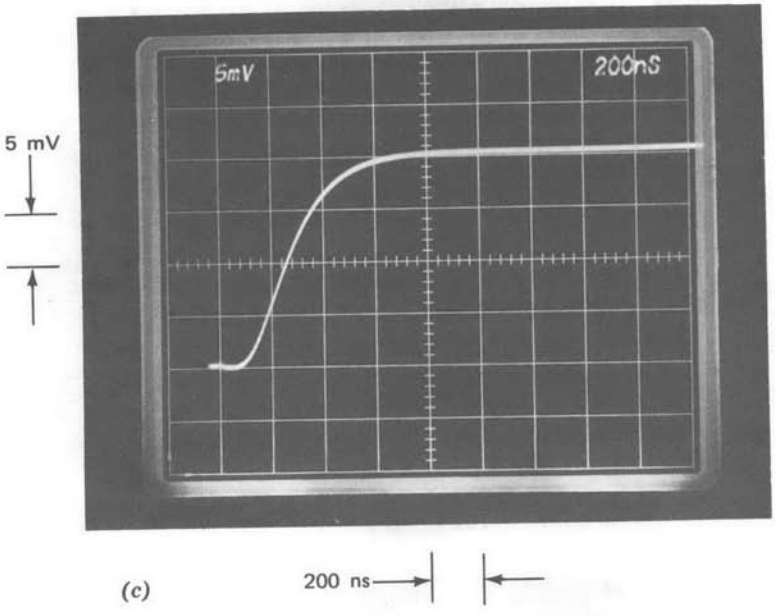


Figure 9.11—Continued

The step response shown in Fig. 9.11 shows how this design allows the effects of changing attenuation inside the loop to be offset by altering compensation. While the attenuation is changed by changing the value of R in this demonstration, it depends on the ideal closed-loop gain in many practical connections. Figure 9.11*a* shows the step response for $\alpha = 1/2$ ($R = \infty$) and $C_c = 20$ pF. The response for $\alpha = 1/4$ ($R = \frac{1}{2}R_1$) and $C_c = 20$ pF is shown in Fig. 9.11*b*. The rise time is approximately twice as long in Fig. 9.11*b*, anticipated since the crossover frequency is a factor of two lower in this connection (see Fig. 9.9). The crossover frequency can be restored to its original value by lowering C_c to 10 pF. The transient response for this value of compensating capacitor (Fig. 9.11*c*) is virtually identical to that shown in part *a* of this figure.

Figure 9.12 demonstrates the slew rate of the amplifier by showing its slew-rate limited response to 20-volt peak-to-peak square wave signals. The parameter values for Fig. 9.12*a* are $\alpha = 1/2$ and $C_c = 20$ pF, while those of Fig. 9.12*b* are $\alpha = 1/4$ and $C_c = 10$ pF. These are the values that gave the virtually identical small-signal responses shown in Figs. 9.11*a* and 9.11*c*, respectively. The large-signal responses show that the slew rate is inversely proportional to compensating-capacitor value, as predicted in Section 9.3.2.

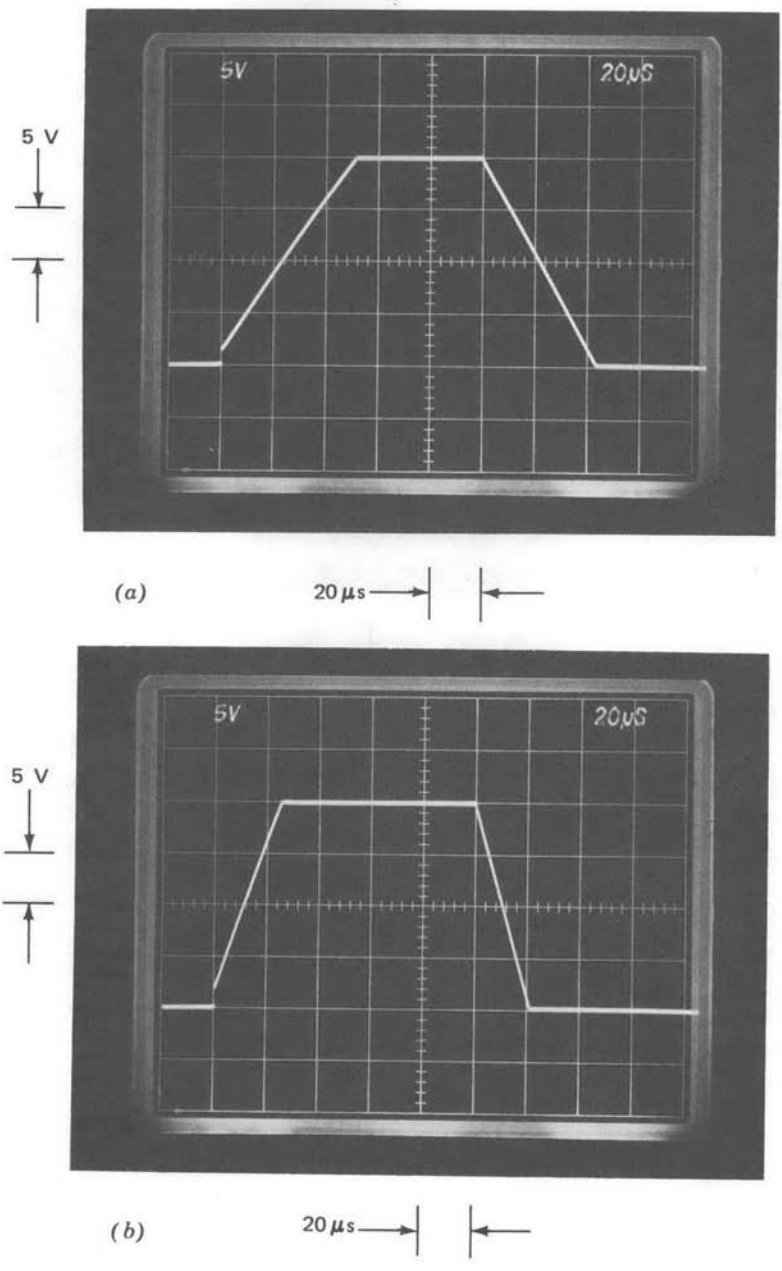


Figure 9.12 Effect of compensating capacitor on large-signal response (input square-wave amplitude is 20 volts peak-peak). (*a*) $C_c = 20$ pF, $\alpha = 1/2$. (*b*) $C_c = 10$ pF, $\alpha = 1/4$.

PROBLEMS

P9.1

Figure 9.13 shows schematics for several available integrated circuits. Determine the transistors that actually contribute to signal amplification for each of these circuits.

P9.2

Assume that measurements made on an operational amplifier of the type described in this chapter indicate a bias current required at either input terminal equal to $9 \times 10^{-4}\text{A}/T^2$, where T is the temperature in degrees Kelvin. We intend to use the amplifier connected for a noninverting gain of two. Design a temperature-dependent network that can partially compensate the input current seen at the noninverting input of the amplifier. Note that since an input voltage range of ± 5 volts is anticipated, the incremental resistance of the compensating source must be the order of $10^{10}\ \Omega$ to achieve good compensation.

P9.3

The input transistors of the amplifier described in this chapter are matched such that the difference between the base-to-emitter voltages of these two devices is less than 3 mV when they operate at equal collector currents. Assume that this matching is not performed, and consequently that the base-to-emitter voltage of Q_2 (see Fig. 9.1) is 50 mV lower than that of Q_1 when the two devices operate at equal currents. The amplifier can still be balanced by replacing the collector-circuit resistor network of the pair with a 650-kΩ potentiometer, and possibly changing the 33-kΩ resistor in the emitter circuit of the Q_4-Q_5 pair so that the quiescent operating level of these devices remains 50 μA following balancing. Calculate the effect that balancing an amplifier with this degree of mismatch between input devices has on the open-loop gain of the amplifier.

P9.4

Figure 9.14 shows a simplified representation for an operational amplifier. You may assume that the current sources have infinite output impedance and that the buffer amplifier has infinite input resistance. All transistors are characterized by $\beta = 200$ and $\eta = 5 \times 10^{-4}$.

(a) Estimate the low-frequency open-loop gain of this configuration.
(b) What is the input offset voltage of the amplifier, assuming that the two input transistors have identical values for I_S?
(c) What is the common-mode rejection ratio of this amplifier?
(d) Estimate the time constant associated with the dominant amplifier pole, assuming all transistors have $C_\pi = 10$ pF, $C_\mu = 5$ pF.
(e) Suggest at least three circuit changes (aside from simply using better transistors) that can increase the value of the d-c open-loop gain.

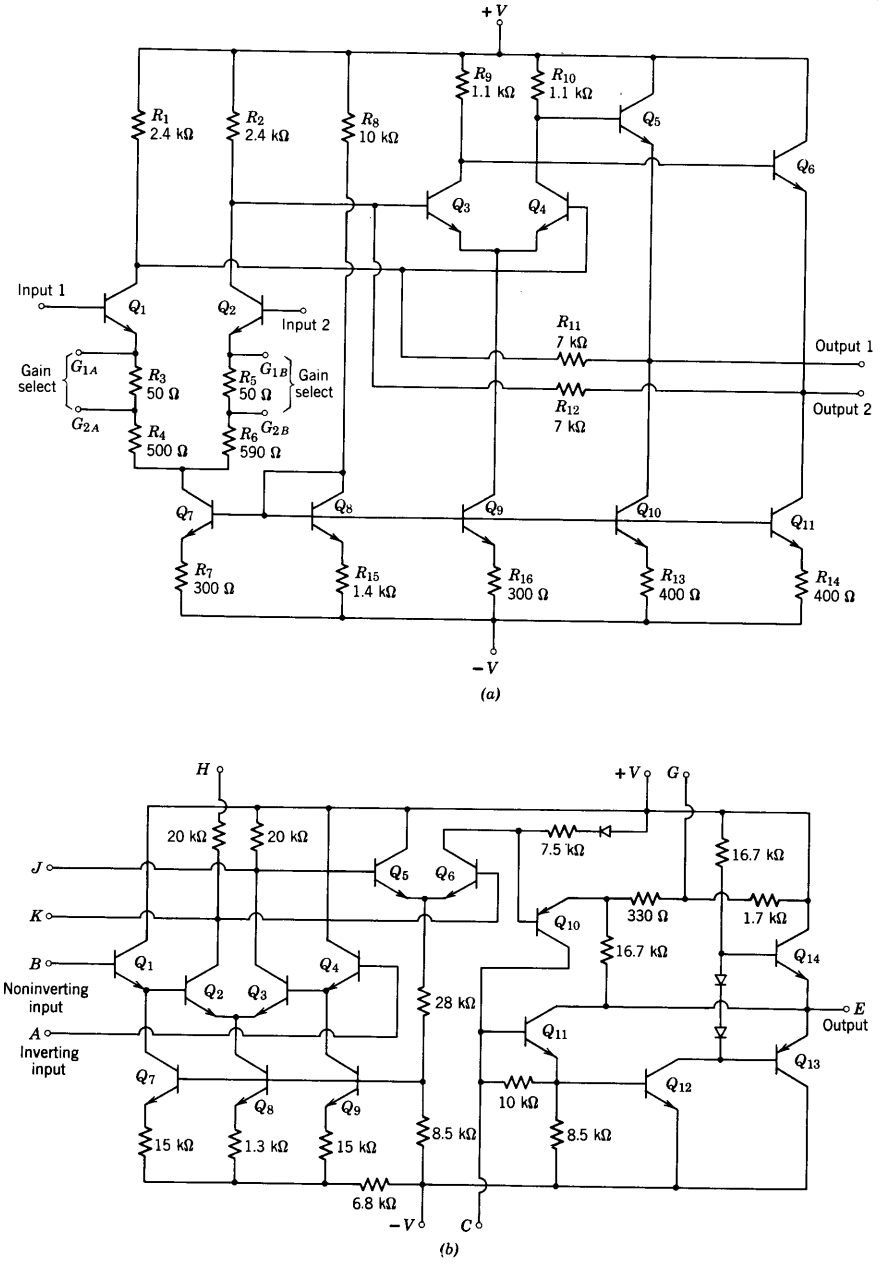
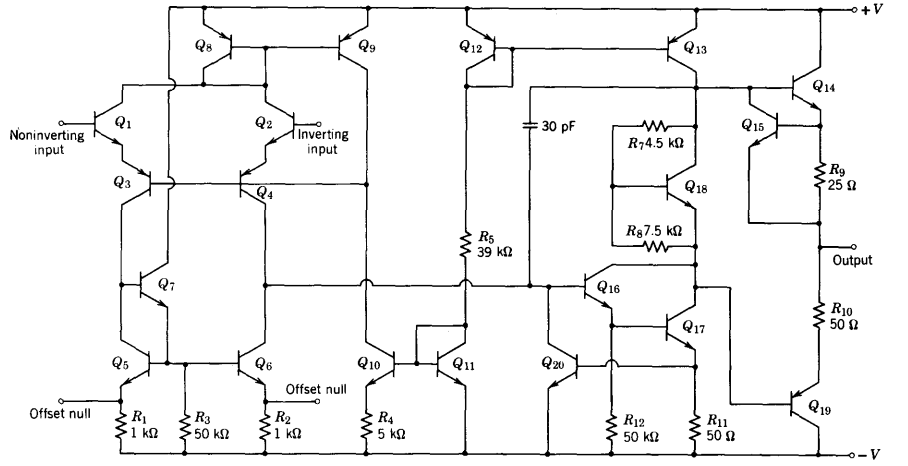
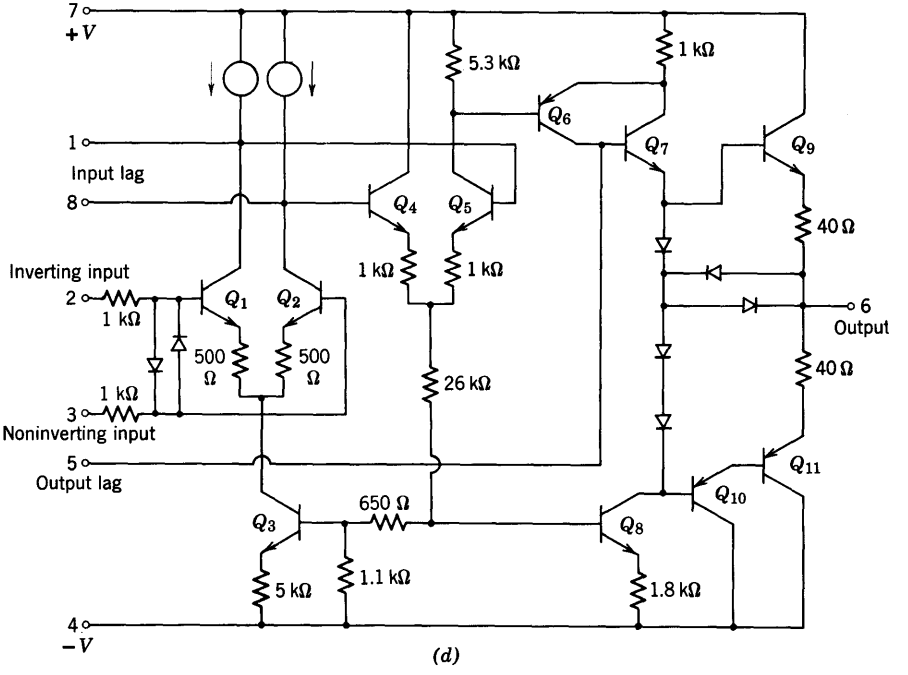


Figure 9.13 Integrated-circuit amplifiers. (*a*) μA733. (*b*) MC1533. (*c*) μA741. (*d*) MC1539.



(c)



(d)

Figure 9.13—Continued

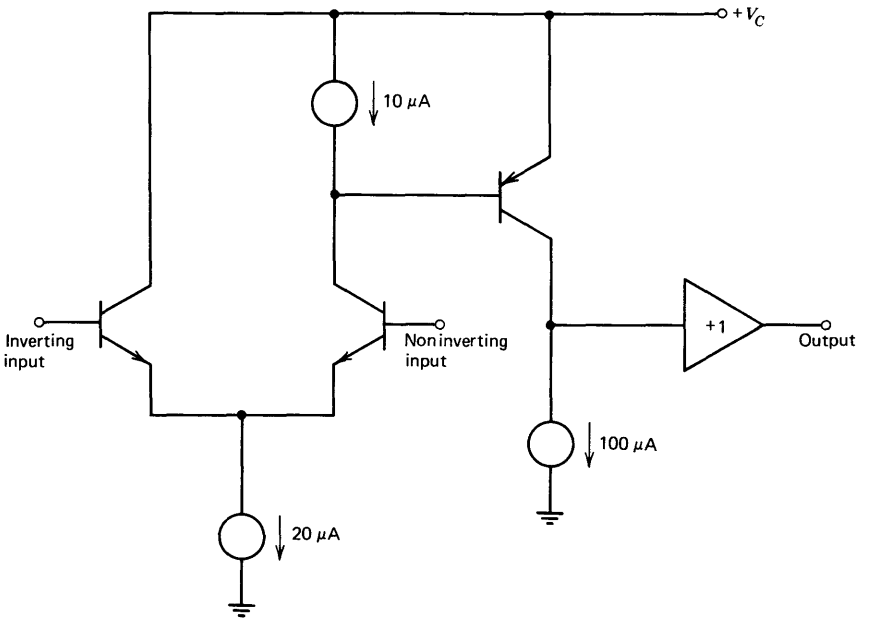


Figure 9.14 Operational amplifier.

P9.5

An interesting amplifier topology that can be used for operational amplifiers intended to be connected as unity-gain voltage followers is shown in Fig. 9.15. (Note that the amplifier is shown connected as a voltage follower.) You may assume that the current sources have infinite output impedance and that all transistors are characterized by $\beta = 100$ and $\eta = 2 \times 10^{-4}$.

(a) How many voltage-gain stages does this amplifier have?

(b) Estimate the unloaded, low-frequency open-loop gain of the amplifier.

(c) Estimate the low-frequency closed-loop output impedance of the circuit.

P9.6

Assume that the field-effect transistor (Q_8 in Fig. 9.1) in the amplifier described in this chapter is replaced with a 2N3707. Use values given in Table 9.1, with appropriate modifications reflecting operation at 2 mA, to determine values for g_m, r_π, r_o, and r_μ. You may assume that the value of C_π at 2 mA is 50 pF. Determine the changes in amplifier d-c open-loop gain and the changes in uncompensated dynamics that result from this design change.

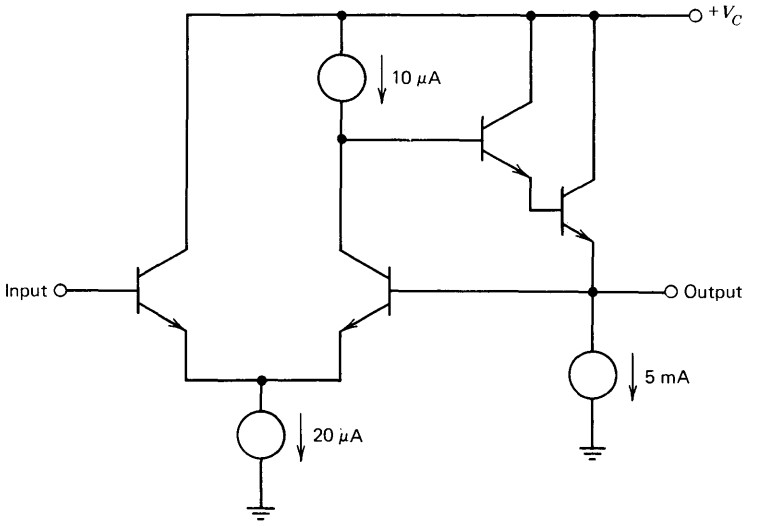


Figure 9.15 Follower-connected amplifier.

P9.7

A detailed analysis of a certain operational amplifier shows that its open-loop transfer function contains a single low-frequency pole, and that the location of this pole is easily controlled by appropriate compensation. In addition to this dominant pole, the open-loop transfer function includes 7 poles at $s = -10^8$ sec^{-1} and two right-half-plane zeros at $s = 2 \times 10^8$ sec^{-1}. Show that, at least at frequencies up to several megahertz, the net effect of these higher-frequency singularities can be modeled as a single time delay. Determine the delay time of an approximating transfer func-

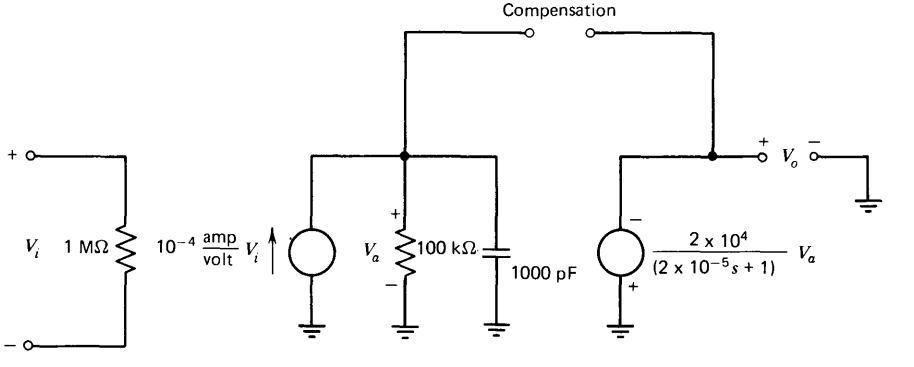


Figure 9.16 Operational-amplifier model.

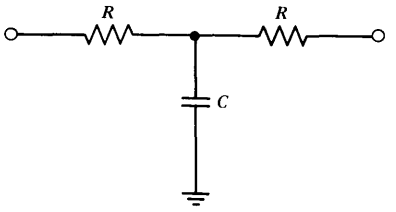


Figure 9.17 Low-pass T network.

tion. Use the time-delay approximation to describe the effect of the higher-order singularities on the maximum crossover frequency of feedback connections that include this amplifier inside the loop. If the d-c open-loop gain of the amplifier is 10^5, how should the dominant pole be located in order to achieve 45° of phase margin when the amplifier is connected as a unity-gain inverter?

P9.8

A model for an operational amplifier is shown in Fig. 9.16. This amplifier is connected as a unity-gain voltage follower.

(a) What is the phase margin with no compensation?
(b) If a capacitor is used between the compensating terminals, how large a value is required to double the uncompensated phase margin?
(c) How large a capacitor should be used to obtain 45° of phase margin in the follower connection?
(d) An alternative compensating technique involves shunting a series R-C network across the 100-kΩ resistor and 1000-pF capacitor combination shown in Fig. 9.16. Find parameter values for this type of compensation that yields results similar to those obtained in part c.

P9.9

The amplifier described in Problem P9.8 is used in a loop where an approximate open-loop transfer function of $10\ (10^{-2}s + 1)$ is required. It

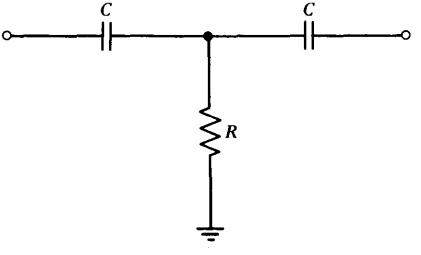


Figure 9.18 High-pass T network.

is suggested that the required transfer function be obtained by compensating the amplifier with the T network shown in Fig. 9.17. Determine network-parameter values that might reasonably be expected to approximate the required transfer function.

When the amplifier is tested with this type of compensation, we find that our first guess was incorrect. Explain.

P9.10

Another class of application involves the use of the T network shown in Fig. 9.18 to compensate the amplifier described in Problem P9.8. This network can be used without encountering the type of difficulties that occur using the network described in Problem P9.9. Determine the type of transfer function that results using the high-pass T, and comment on the value of this type of compensation.

P9.11

It was mentioned in Section 9.3.1 that the temperature stability of the amplifier described in this chapter could be improved by making the bias current source of the first stage have an output current directly proportional to temperature. This proportionality can be accomplished by means of the circuit shown in Fig. 9.19. Assume that the transistor current-voltage characteristic is

$$i_C = AT^3 \, e^{q(V_{BE}-V_{go})/kT}$$

Determine the value of V_B that results in an output current directly proportional to temperature at 300° K.

P9.12

A two-stage operational amplifier can be modeled as shown in Fig. 9.20. In this representation, the high-gain second stage itself is modeled

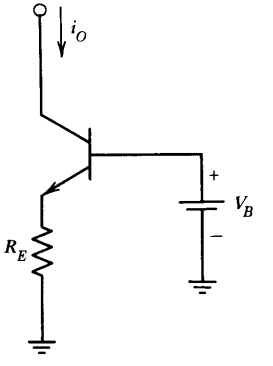


Figure 9.19 Temperature-dependent current source.

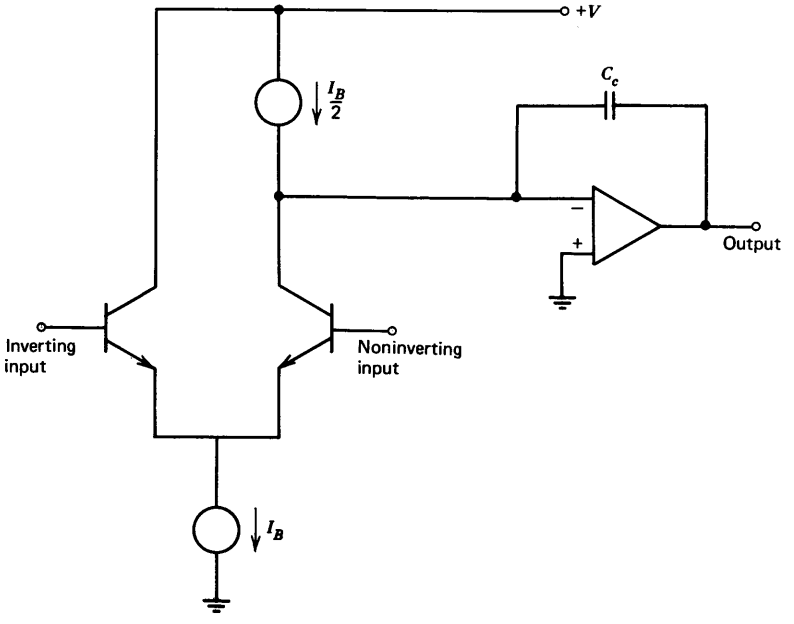


Figure 9.20 Model for two-stage operational amplifier.

as an operational amplifier with a minor-loop feedback element connected around it. You may assume that the second stage has ideal characteristics (i.e., infinite gain and input impedance, zero output impedance, etc.).

(a) Determine the unity-gain frequency of this amplifier as a function of I_B and C_c.
(b) Express the slew rate of the amplifier in terms of the same parameters.
(c) Find a design modification that allows an increase in slew rate without increasing unity-gain frequency.

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