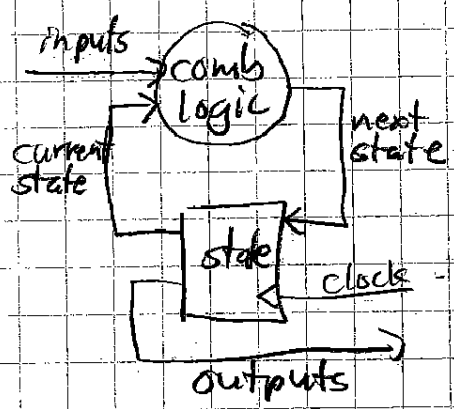


Taxonomy of fixed-connection networks

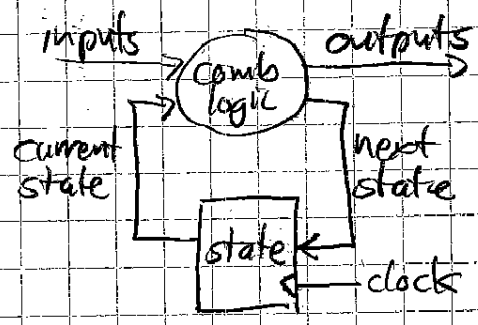
- systolic - all state and interprocessor communication is clocked.
- semisystolic - all state is clocked.
- combinational - no state, no clocks

Finite-state machines

Moore machine



Mealy machine



A systolic network is a network of Moore machines.
 A semisystolic " " " " " Mealy " "
 (with no comb loops).

Example Semisystolic palindrome recognizer

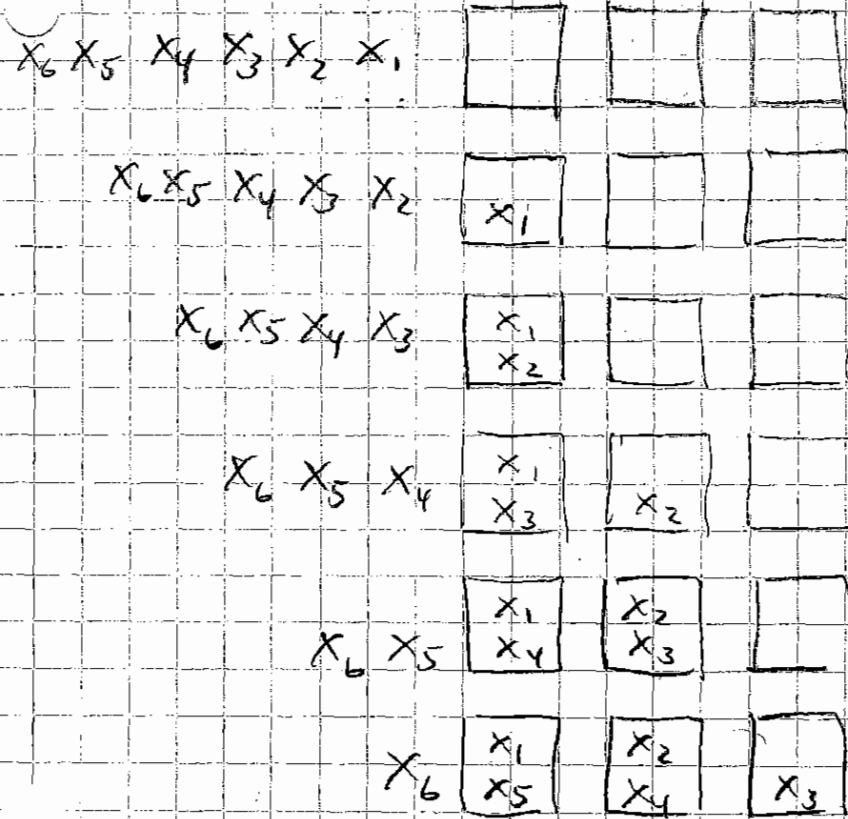
(Palindrome if $x = x^R$ (reverse))

Takes seq. $\langle x_1, x_2, \dots \rangle$ as input. Produces $\langle y_1, y_2, \dots \rangle$ as output, where

$$y_i = \begin{cases} 1 & \text{if } x_1 x_2 \dots x_i \text{ is a palindrome} \\ 0 & \text{otherwise.} \end{cases}$$

E.g. $x = \langle a, b, a, c, a, b, a \rangle$
 $y = \langle 1, 0, 1, 0, 0, 0, 1 \rangle$

Semisystolic network - systolic + global comb logic

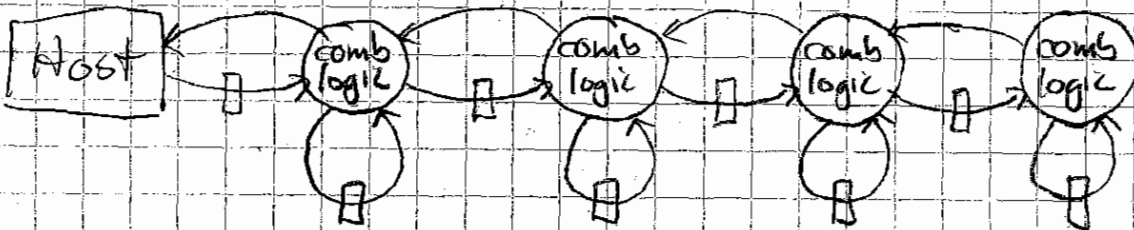


Each cell compares its two values.
Ripple a global AND from right to left.

Real time: On same tick that x_i is input,
 y_i is output.

Only trouble: long clock period.
 $\Theta(N)$ for N -cell array.

Abstract view of circuit

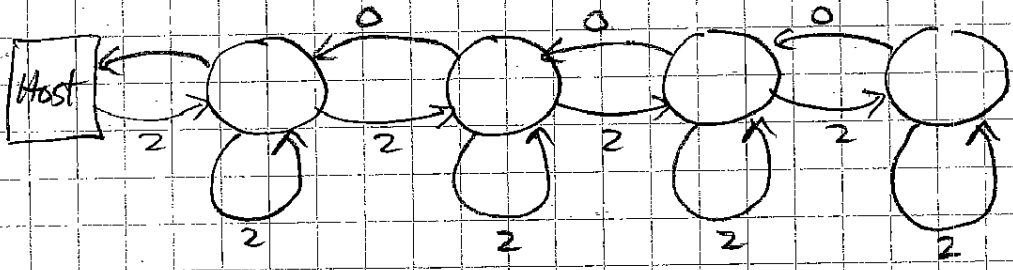


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 L6.3
 + no 0-weight cycles

Semisystolic: ≥ 0 registers on each edge
 Systolic ≥ 1 register on each edge

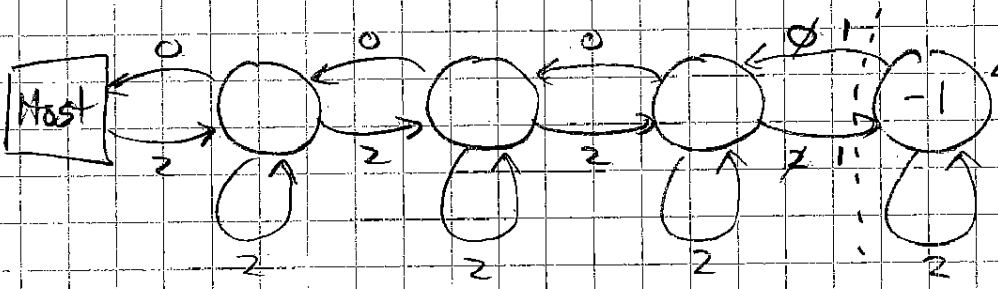
Transformation techniques

1. Slowdown: Double register counts

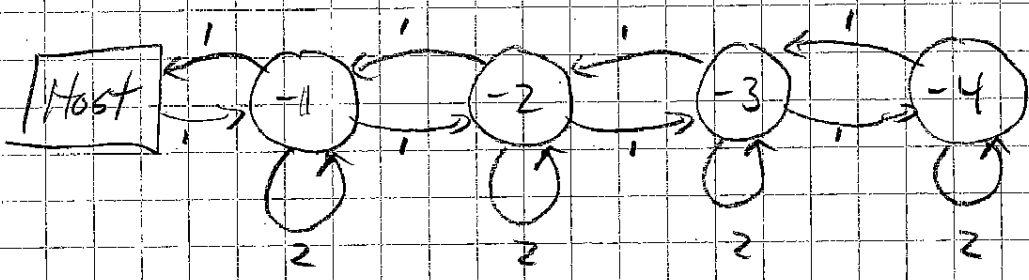


Same function as original semisystolic circuit, but clock twice.

2. Retime



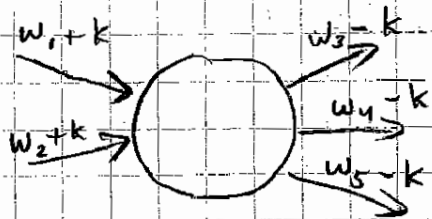
lead of 1
 lag of -1



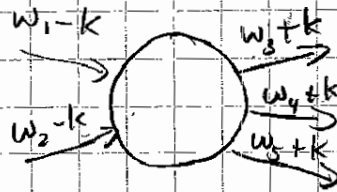
Systolic! Same functionality as doubled semisystolic circuit, but no long comb. delays.
 - Initialization may differ.

Retiming a node

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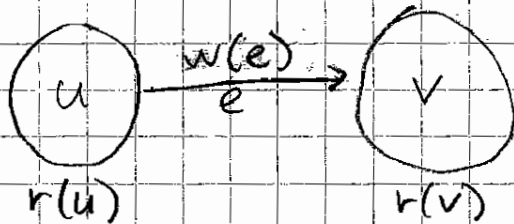


lag of $r(v) = k$



lag of $r(v) = -k$

Retimed edge weights must be ≥ 0 .



$$w_r(e) = w(e) - r(u) + r(v)$$

Def. Let $G = (V, E, w)$ be edge-weighted digraph, where $w(e) \geq 0 \forall e \in E$. A retiming of G is a mapping $r: V \rightarrow \mathbb{Z}$. The retimed graph is $G_r = (V, E, w_r)$, where $w_r(e) = w(e) - r(u) + r(v) \forall e \in E$. The retiming is legal if $w_r(e) \geq 0 \forall e \in E$.

Note: Normally, we assume $r(\text{Host}) = 0$.

Lemma. Let $G = (V, E, w)$ be circuit, and let $r: V \rightarrow \mathbb{Z}$ be retiming. Then, for any path $u \xrightarrow{P} v$ in G , we have

$$w_r(p) = w(p) - r(u) + r(v).$$

Pf. Sup. p is $v_0 \xrightarrow{e_0} v_1 \xrightarrow{e_1} \dots \xrightarrow{e_{k-1}} v_k$.

$$w_r(p) = \sum_{i=0}^{k-1} w_r(e_i)$$

$$= \sum_{i=0}^{k-1} (w(e_i) - r(v_i) + r(v_{i+1}))$$

$$= \sum_{i=0}^{k-1} w(e_i) + \sum_{i=0}^{k-1} (-r(v_i) + r(v_{i+1}))$$

$$= w(p) - r(v_0) + r(v_k) \quad (\text{telescope}) \quad \square$$

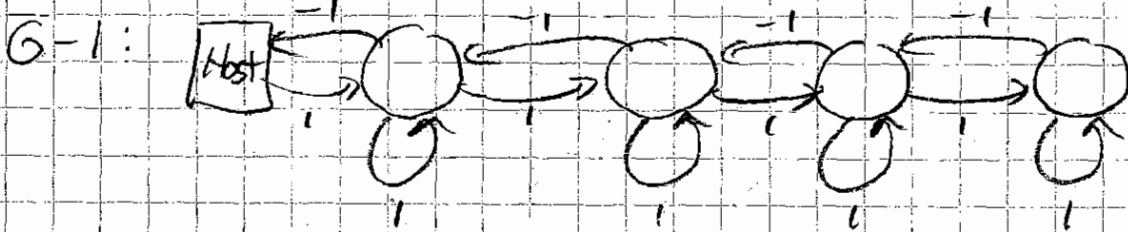
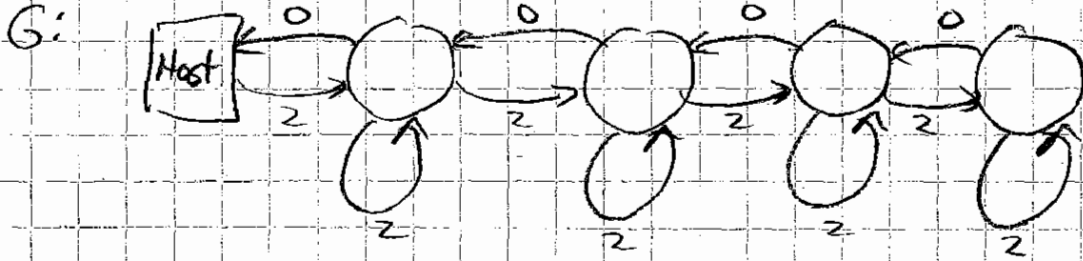
Corollary. For any cycle p , $w_r(p) = w(p)$. \square

Theorem (Systolic conversion)

Let $G = (V, E, w)$ be a semisystolic circuit, and define $G^{-1} = (V, E, w')$, where $w'(e) = w(e) - 1 \forall e \in E$. Then, \exists legal retiming $r: V \rightarrow \mathbb{Z}$ of G such that G_r is systolic iff G^{-1} has no negative-weight cycles.

the "constraint graph"

Example.



No neg-wt cycles.

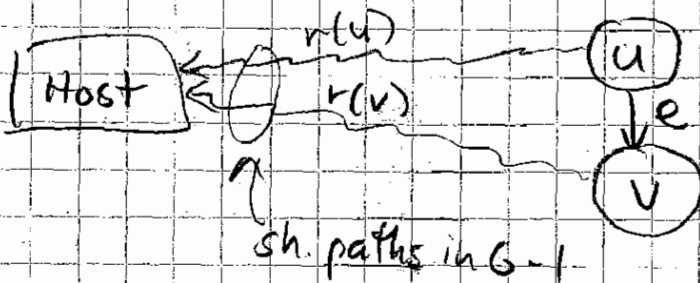
Proof.

(\Leftarrow) Sup. G-1 has no neg-wt cycles.

Define $r(v) =$ wt of shortest path from v to host in G-1

Note: $r(v)$ defined, since G-1 has no neg-wt cycles.

Claim: $\forall u \xrightarrow{e} v \in E, w_r(e) = w(e) - r(u) + r(v) \geq 1.$



$$\Delta\text{-ineq: } \underbrace{r(u)}_{\substack{\text{sh. path} \\ \text{from } u \\ \text{in } G-1}} \leq \underbrace{w(e) - 1}_{\substack{\text{wt. of } e \\ \text{in } G-1}} + \underbrace{r(v)}_{\substack{\text{sh. path} \\ \text{from } v \\ \text{in } G-1}}$$

Rewrite: $w_r(e) = w(e) - r(u) + r(v) \geq 1.$

(\Leftarrow) Sup. $G-1$ has neg.-wt cycle $v_0 \xrightarrow{e_0} v_1 \rightarrow \dots \rightarrow v_k \xrightarrow{e_k} v_0$

$$\text{Then } \sum_{i=0}^k (w(e_i) - 1) < 0$$

$$\Rightarrow \sum_{i=0}^k w(e_i) < k.$$

$$\text{But, } \sum_{i=0}^k w_r(e_i) \geq k, \text{ and } \sum_{i=0}^k w_r(e_i) = \sum_{i=0}^k w(e_i).$$

Contradiction. \square

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L6.7