6.896
4-12-2004
Lecture 16.1
Bradley C. Kuszmaul

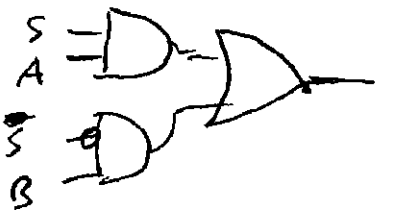
More CMOS circuits

MUX:

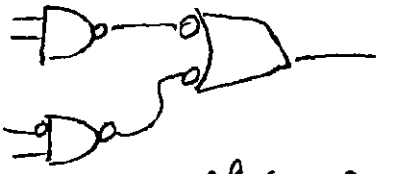
TRUTH TABLE

S	A	B	D
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

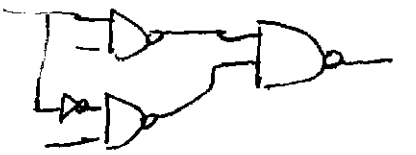
MADE OF GATES



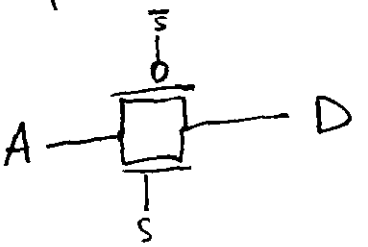
!!! add matched inverters



!!! by Demorgans



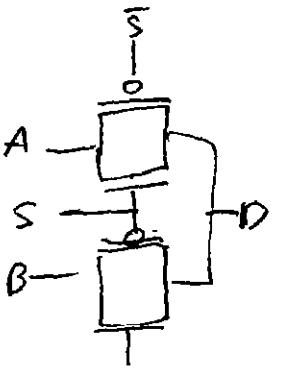
We can implement muxes with pass-~~transistors~~ gates



truth table

~~S~~A	S	A	
~~0~~0	0	0	? } no value provided
0~~1~~1	0	1	?
1~~0~~0	1	0	0 } somewhat weaker
1~~1~~1	1	1	1

MUX



if S is 1 the top pass gate ~~pass~~ allows A through
else the bottom gate lets B through.

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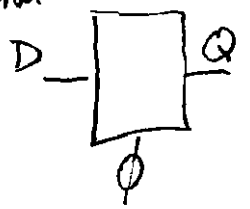
More circuits:

~~Registers + latches~~

STATE:

Level-~~sensitive~~ clocked latches:

Symbol

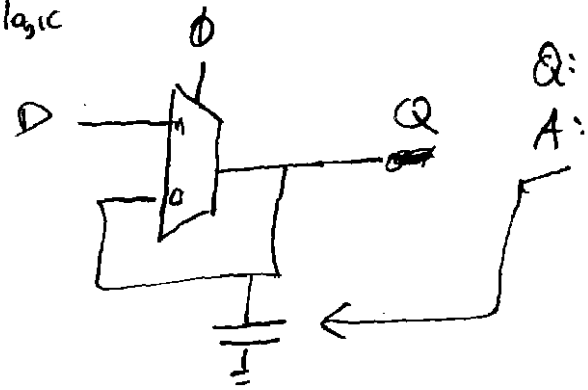


~~Logic~~ Truth Table

D	Φ	Q
0	0	D
1	0	D
X	1	Q

Φ if Φ=0 pass data through
if Φ=1 freeze output

In logic

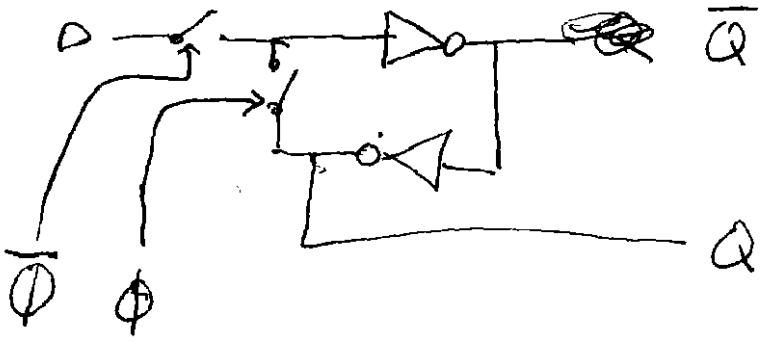


Q: Why does this work?

A: capacitance here holds the old value long enough for the circuit to stay stable when Φ=1

Brief review of EE by analogy to water current
~~electric current~~ ⇔ water current
capacitor ⇔ holding tank
~~resistor~~ ⇔ pipe

Using pass gates



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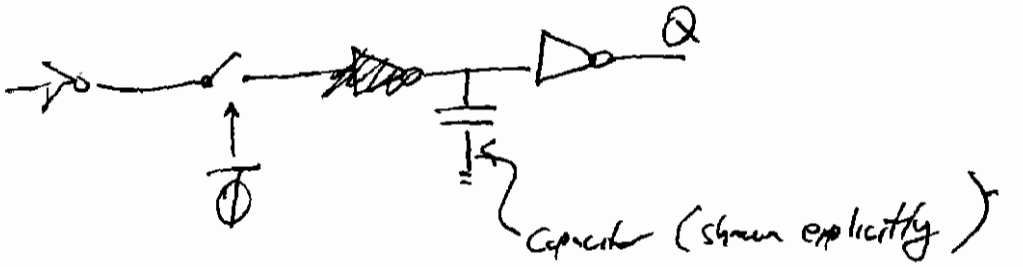
Lecture 16.3

Level sensitive Dynamic Latch.

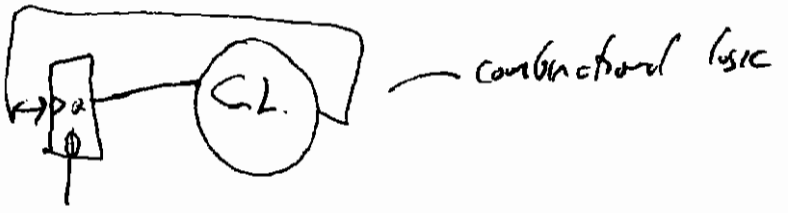
Why better to ~~not~~ "restore" it with feedback?
∃ a capacitor.



Often ∃ a lot of capacitance in ~~circuits~~ CMOS
if Φ runs fast enough (> 1000 Hz e.g.) then this is OK.

Two-phase clocking

Level-sensitive latches are a little tricky — can't make
a state machine with ~~not~~ that can't



when Φ = 0 there is a loop through the C.L.

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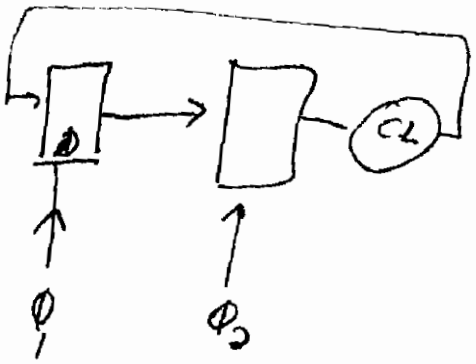
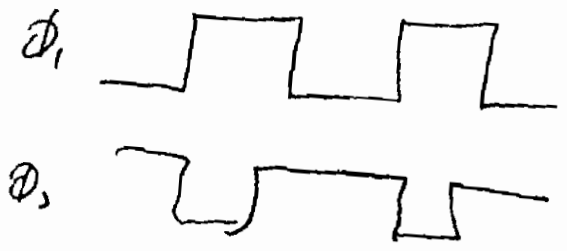
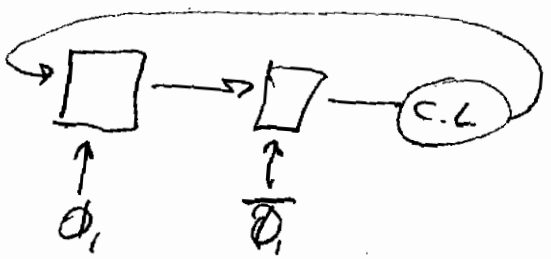
Two phase nonoverlapping clocks





ϕ_1 ~~don't~~ low + ϕ_2 low don't happen at the same time

When ϕ_1 is low data passes through first latch, + ϕ_2 holds its old value.
Then when ϕ_2 is low, ϕ_1 is up, so it holds the value coming out of C.L., and data flows through ϕ_2



Will this work?
What if $\overline{\phi_1}$ and ϕ_1 get a little misaligned so they low parts overlap?

It is ok. if the C.L. has a long enough ~~delay~~ contamination delay.

Or if you arrange $\overline{\phi_2}$ to be non-overlapping

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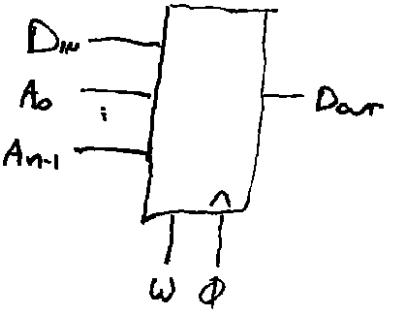
RAM

Random Access Memory



An array of $N=2^n$ bits

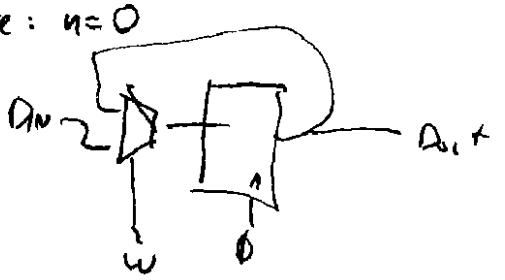
$A_0, \ldots, A_{n-1}$ names the bit B_i

at Φ↑ if W then write D_{IN} to B_i

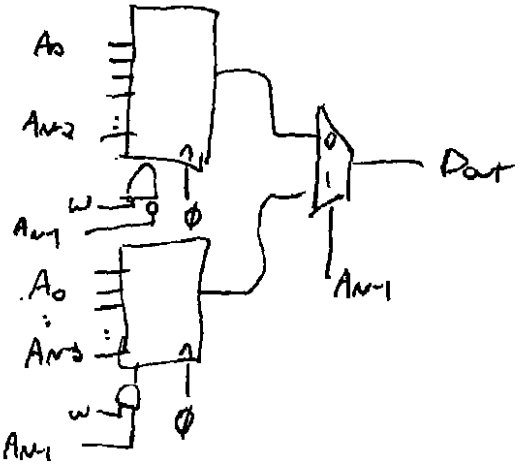
else $D_{OUT} = B_i$

Divide and Conquer

Base case: $n=0$



$n>0$



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Analysis of RAM

Critical path:

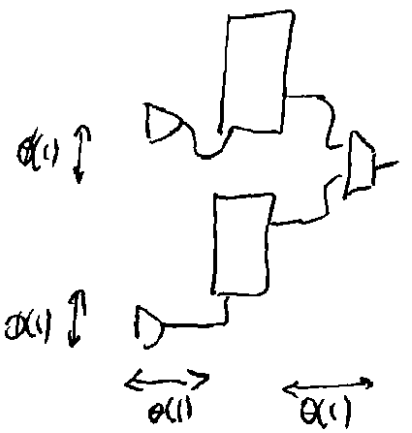
$$T(0) = \Theta(1)$$

$$T(n) = 1 \text{ gate} + 1 \text{ mux} + T(n-1)$$

$$= \Theta(n)$$

$$= \Theta(\log N)$$

Area: Need a layout



width:

$$W(n) = \Theta(1) + W(n-1)$$

$$= \Theta(n) = \Theta(\log N)$$

height

$$H(n) = \Theta(1) + 2 \cdot H(n-1)$$

$$= \Theta(2^n) = \Theta(N)$$

Q: Can we do better?

A: Yes

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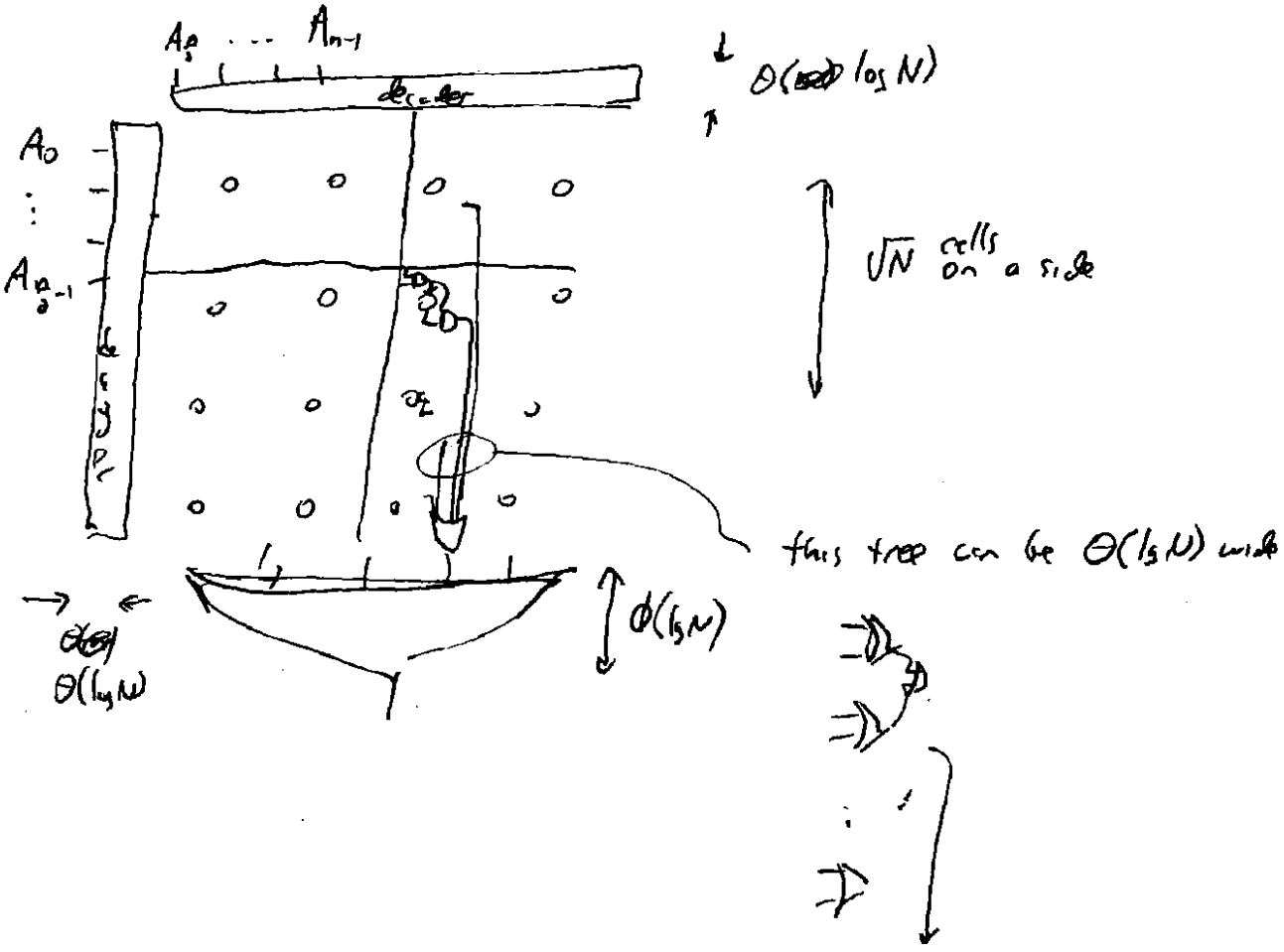

total access width:

$$\Theta(\lg N) + \Theta(\sqrt{N} \cdot \lg N)$$

total height

$$\Theta(\lg N) + \Theta(\sqrt{N})$$

total area = $\Theta(N \lg N)$ not better yet!

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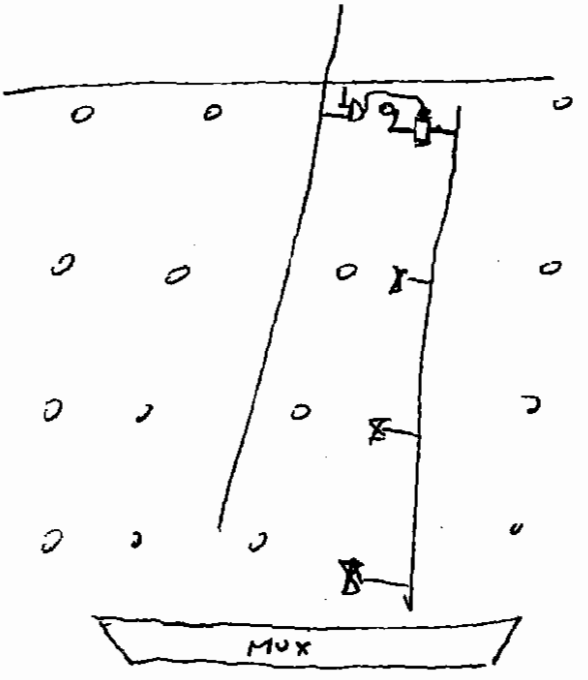
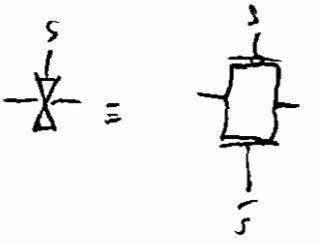
But for small N we do "wired or"





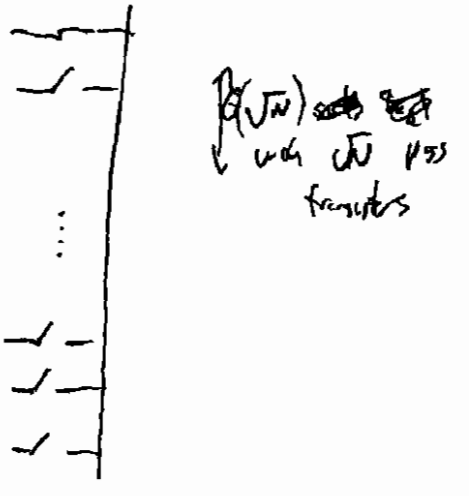
width = $\Theta(\sqrt{N})$
area = $\Theta(N)$

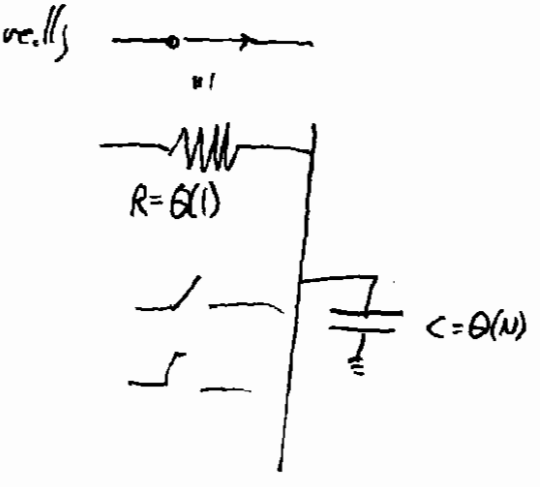
two issues:

Q1) if no one drives the line, what happens?

A: Don't care. The MUX doesn't look at it.

Q2: performance: to drive a long wired or takes time.





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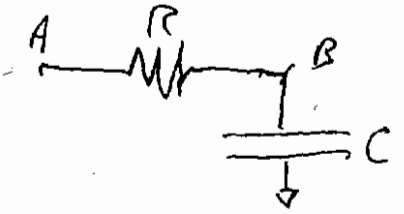
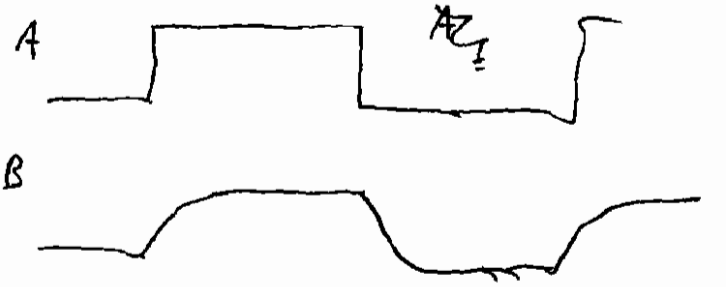
"Now we need to understand RC circuits"

RC circuits





two properties of electricity
current (AMPS) (V) [think current of water in a pipe]
~~voltage~~
potential (VOLTS) (I) [think pressure of water in pipe]

Resistor: $V = I \cdot R$ or $\frac{V}{R} = I$ (more flow if you push harder)

Capacitor: $\int I\,dt = V \cdot C$ (as you pump current through, the voltage goes up)

$= I = \frac{dV}{dt} \cdot C$

OR RC circuit

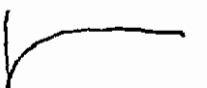
~~$\int I\,dt = I \cdot C$~~ $V = \frac{dV}{dt} \cdot RC$

this is a differential equation with solution of the form

$V = e^{t/RC} + b$ for some τ and b

$e^{t/\tau} + b = \frac{1}{\tau} e^{t/\tau} \cdot RC$

$\Rightarrow \tau = RC$ τ is the "time constant" for the RC circuit



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So our circuit has

$R = \Theta(1)$

$C = \Theta(b \cdot \sqrt{N})$

So $\tau = \Theta(\sqrt{N})$

Next time we'll improve on this