# 6.302 Feedback Systems

Recitation 11: Phase-locked Loops

Prof. Joel L. Dawson

Phase-locked loops are a foundational building block for analog circuit design, particularly for communications circuits. They provide a good example system for this class because they are an excellent exercise in physical modeling. In these systems, the key variable is the phase of a sinusoid. As a first step, then we must be precise about what we mean by the phase of a sinusoid. Consider:

$$v(t) = \cos[\phi(t)]$$

We define the frequency of a sinusoid as the instantaneous rate of change of its phase. That is:

$$\omega \equiv \frac{d\phi}{dt}$$

EXAMPLE: $v(t) = \cos(\omega_0 t + \phi_0)$

PHASE = $\omega_0 t + \phi_0 = \phi(t)$

FREQUENCY = $\dfrac{d\phi(t)}{dt} = \omega_0$

To be consistent, we write the phase in terms of the frequency:

$$\phi = \int_{-\infty}^{t} \omega(t)\,dt$$

So to understand phase-locked loops (PLLs) we must make the following conceptual jump...

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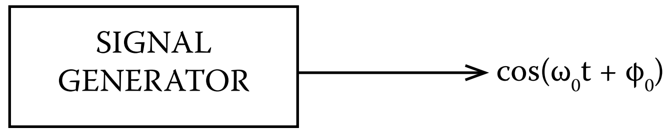
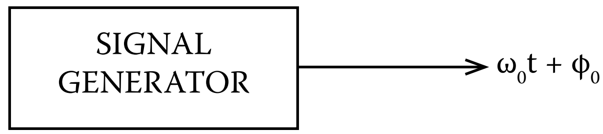
VOLTAGE PICTURE:

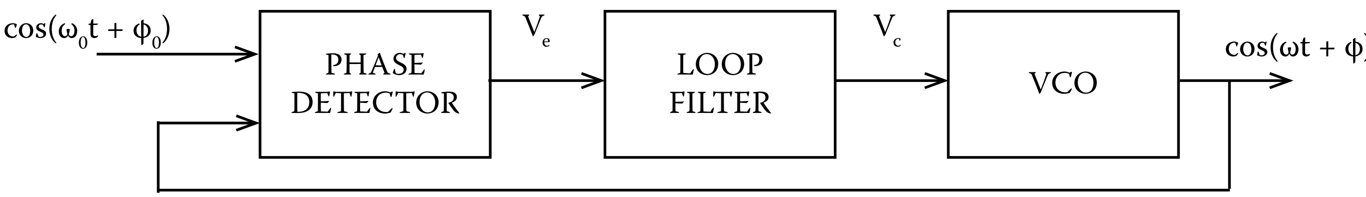



PLL PICTURE:




Now, the anatomy of a PLL:

VOLTAGE PICTURE




VCO = Voltage Controlled Oscillator

$\omega = k_0 V_c$

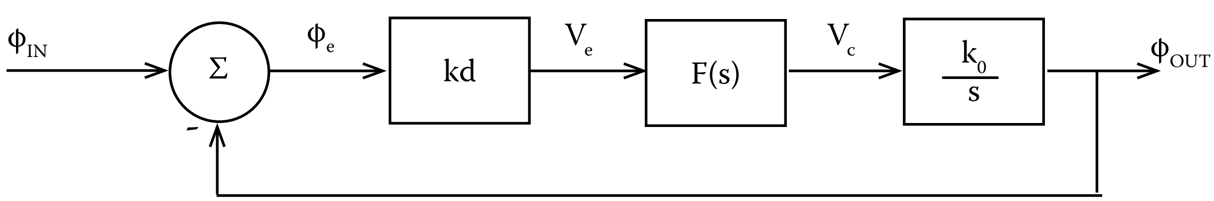
$V_e = k_d (\phi_0 - \phi)$

$[kd] = {}^{V}/_{RAD}$

Notice, if $V_e$ is constant, $\phi - \phi_0$ is constant => $\omega_0 = \omega$

A PLL locks the output of a VCO in frequency and phase to an incoming periodic signal.

PLL PICTURE




VCO is an integrator. Its output frequency is

$$\frac{d\phi_{OUT}}{dt} = k_0 V_c \Rightarrow \phi_{OUT} = \int_{-\infty}^{t} k_0 V_c \, dt$$

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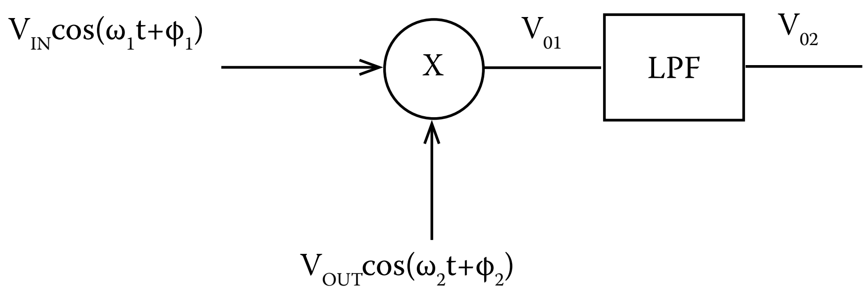
Now, let's look at how we put together and use PLLs. To start, how does one build a phase detector?

1) ANALOG MULTIPLIER:




$$V_{01} = V_{IN}V_{OUT}\cos(\omega_1 t+\phi_1)\cos(\omega_2 t+\phi_2)$$

$$= \tfrac{1}{2} V_{IN}V_{OUT}\left[\cos(\omega_1 t + \phi_1 + \omega_2 t + \phi_2) + \cos(\omega_1 t + \phi_1 - \omega_2 t - \phi_2)\right]$$

IF $\omega_1 = \omega_2 = \omega$

$$V_{01} = \tfrac{1}{2} V_{IN}V_{OUT}\left[\cos(2\omega t + \phi_1 + \phi_2) + \cos(\phi_1 - \phi_2)\right]$$

After LPF, we lose high-frequency component:

$$V_{02} = \tfrac{1}{2} V_{IN}V_{OUT}\left[\cos(\phi_1 - \phi_2)\right]$$

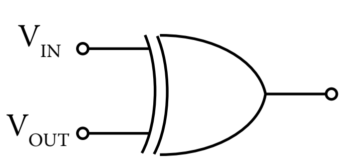
So we get zero out of the phase detector when $\phi_1 - \phi_2 = \pm {}^{\pi}/_{2}$ .

Linearizing about this condition, we would say:

$$\Delta v_{02} = \pm \underbrace{\frac{V_{IN}V_{OUT}}{2}}_{k_0} \Delta\phi$$

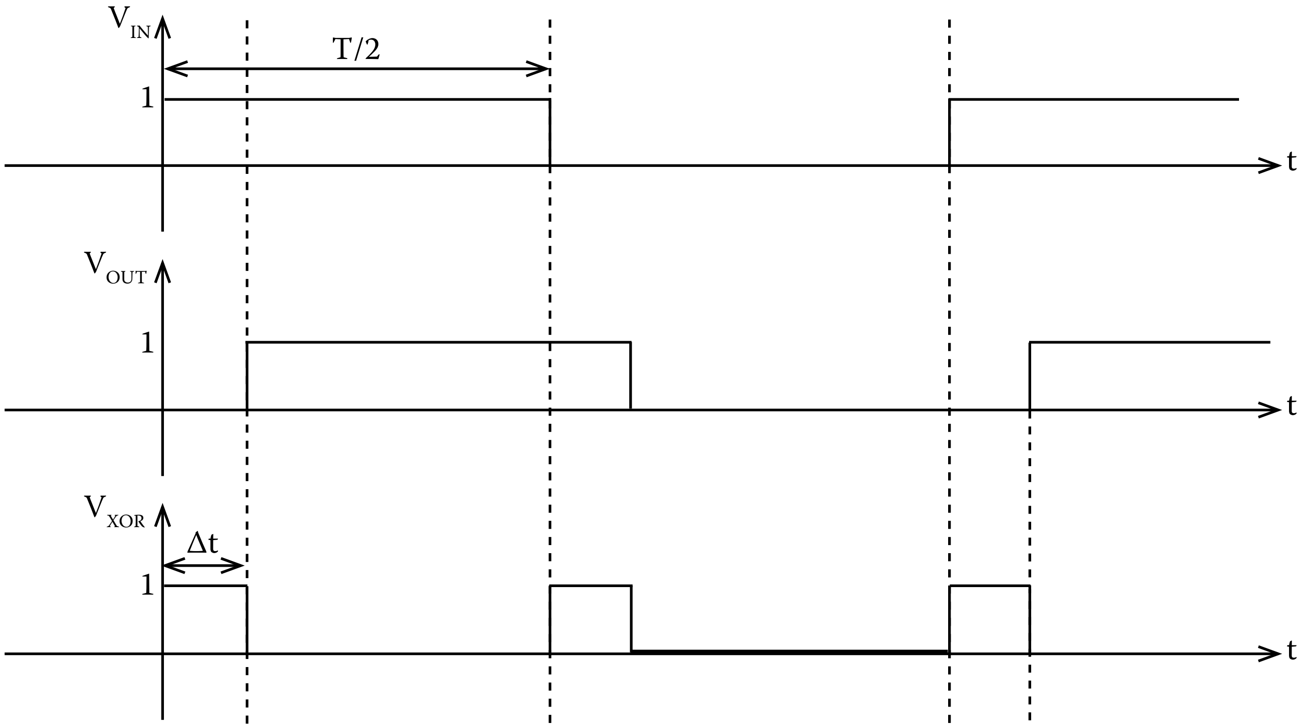
(Notice that the constant $k_0$ depends on the amplitude of the sinusoids.)

2) DIGITAL XOR GATE




| $V_{IN}$ | $V_{OUT}$ | $V_{XOR}$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Easiest to analyze in time domain. (Here, assume square wave inputs.)




For our phase detector output, we'll use the average (DC) value of $V_{XOR}$:

$$\overline{V}_{XOR} = \frac{1}{T/2}\left[1\cdot\Delta t + 0\cdot\left({}^{T}/_{2} - \Delta t\right)\right] = 2\cdot\frac{\Delta t}{T}$$

Now, how do we relate this to phase? Recall that for a sinusoid:

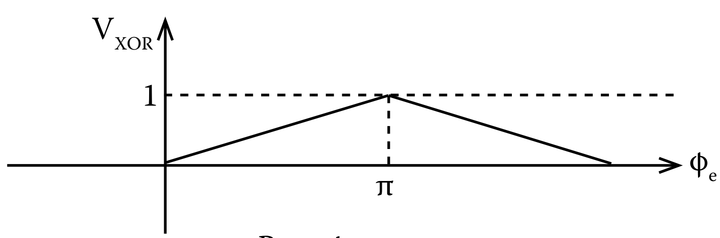
$$\cos(\omega t - \phi) = \cos(2\pi f t - \phi)$$

$$= \cos\left(\frac{2\pi}{T} t - \phi\right)$$

$$= \cos\frac{2\pi}{T}\left(t - \frac{\phi}{2\pi}\cdot T\right)$$

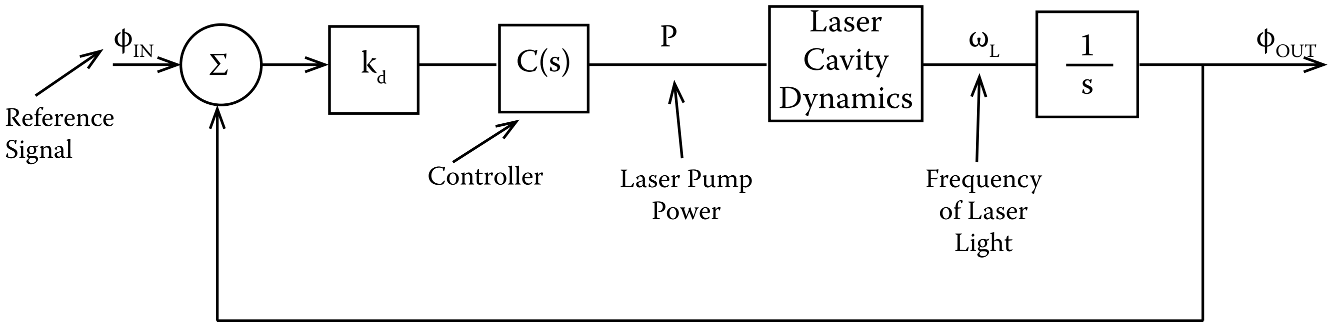
$$= \cos\frac{2\pi}{T}(t - \Delta t) \Rightarrow \Delta t = \frac{\phi}{2\pi}\cdot T$$

THUS: $\overline{V}_{XOR} = \frac{\cancel{2}}{\cancel{T}}\left(\frac{\phi_e}{\cancel{2}\pi}\cdot\cancel{T}\right) = \frac{\phi_e}{2\pi}$



There are many other phase detectors, each with their own strengths and weaknesses. More on these later...

Application to stabilization of the frequency of a laser




Locks frequency of laser light to a stable reference.

Typical laser cavity dynamics:

$$G(s) = \underset{\text{delay}}{e^{-ST}} \underbrace{\frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}}_{\text{second order system}}$$

Typical choices for a controller: $C(s) = D_0 s$
$D_0 s + P_0$
$I_0 \frac{1}{s}$

Returning to a general case, we have $L(s) = \frac{k_0 k_d}{s}$ F(s), where as a designer you usually have some control over the form of F(s). Suppose we choose F(s) = 1, so that L(s) is just $\frac{k_0 k_d}{s}$ . What is the steady-state error in response to a constant-frequency input?

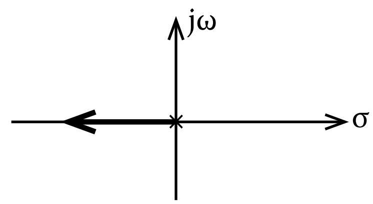
$$\cos(\omega_0 t) \longrightarrow \text{ramp in phase} \longrightarrow \frac{\omega_0}{s^2}$$

Steady-state error, then, is

$$\lim_{t \to \infty} \phi_e(t) = \lim_{s \to 0} s\left[\frac{\omega_0}{s^2} \cdot \frac{1}{1+C(s)}\right] = \lim_{s \to 0} \frac{\omega_0}{s} \frac{1}{1+\frac{k_0 k_d}{s}}$$

$$= \frac{\omega_0}{k_0 k_d}$$

=> Large $k_0k_d$ for small phase error. But according to root locus,

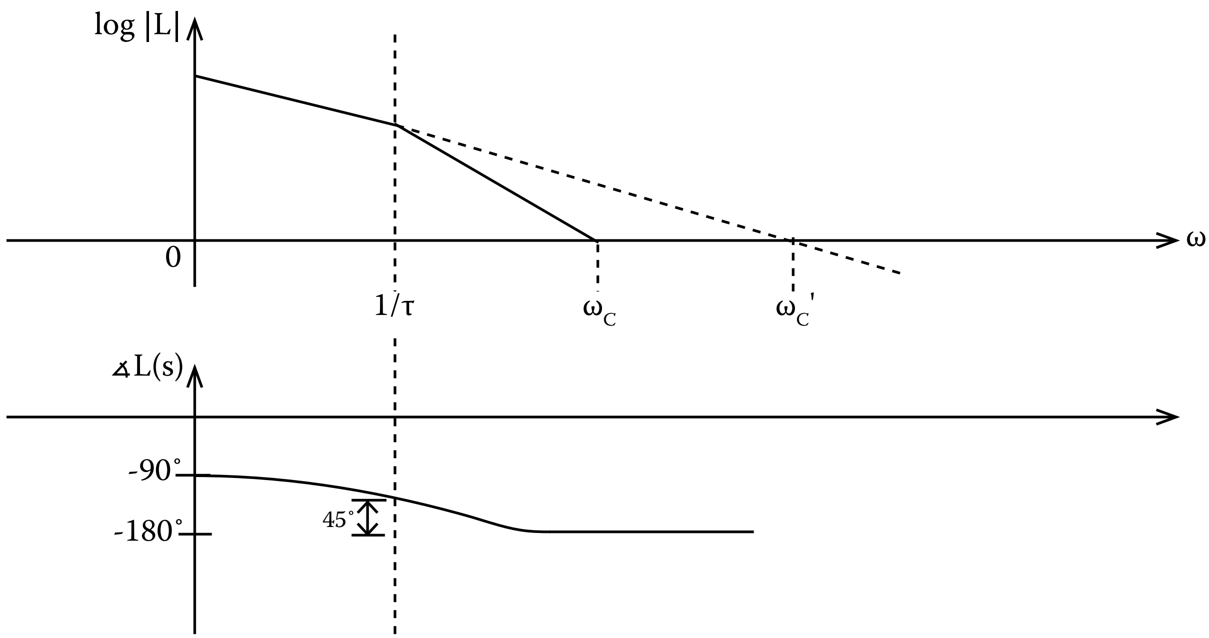



Large $k_0k_d$ also means large bandwidth. If we have a noisy reference, large bandwidth is not a good thing.

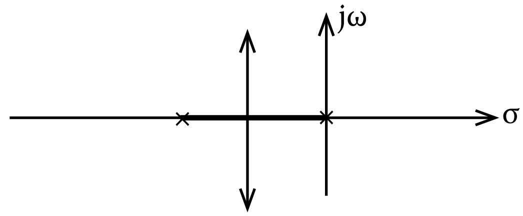
We can improve things by being more sophisticated in our choice of F(s):

$$F(s) = \frac{1}{\tau s + 1} \quad => \quad L(s) = \frac{k}{s(s\tau + 1)}$$

Steady state error is still $\frac{\omega_0}{k}$, but bandwidth is reduced:



Now we've got our improved noise performance, but increasing k will lower our damping ratio:




Put another way, increasing k will lower our phase margin.
=> we must decide what stability margins are acceptable in our application.

Suppose we decide that a 25% overshoot in the step response is acceptable. Using our chart of 2ns order parameters, we discover that this corresponds to $\zeta = 0.4$ and $M_p = 1.4$. This means we should design for a phase margin of

$$M_p \approx \frac{1}{\sin\phi_m}$$

$$\phi n \approx \sin^{-1}\left(\frac{1}{m_p}\right) \approx 45^\circ$$

We arrange for this by ensuring that $|L| = 1$ at the frequency for which $\measuredangle L(s) = -135^\circ$. Looking at our Bode Plot, we see that this frequency is just $\omega = 1/\tau$. On the asymptotic magnitude plot, $|L(s)|$ at this frequency is $\frac{k}{1/\tau} = k\tau$. The actual magnitude is $\frac{k\tau}{\sqrt{2}}$ .

We therefore choose k using

$$\frac{k\tau}{\sqrt{2}} = 1 \Rightarrow k = \frac{\sqrt{2}}{\tau}$$