

6.301 Solid State Circuits

Fall Term 2010
Problem Set 3

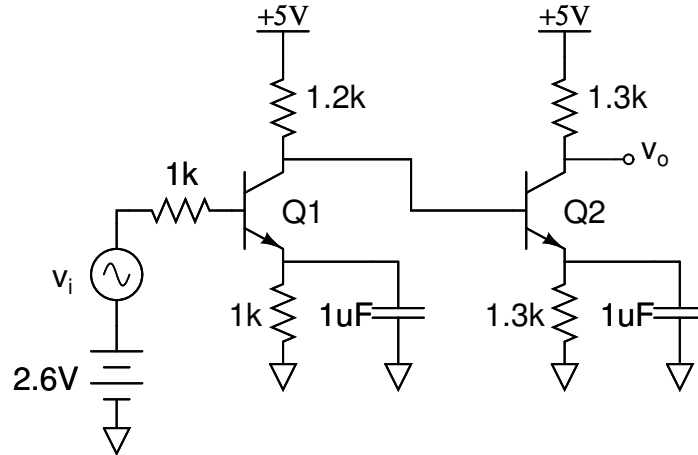
Issued : Sept. 17, 2010
Due : Friday, Sept. 24, 2010

Suggested Reading: Read as many of the following as you can. All of the recommended references are on reserve at Barker Library.

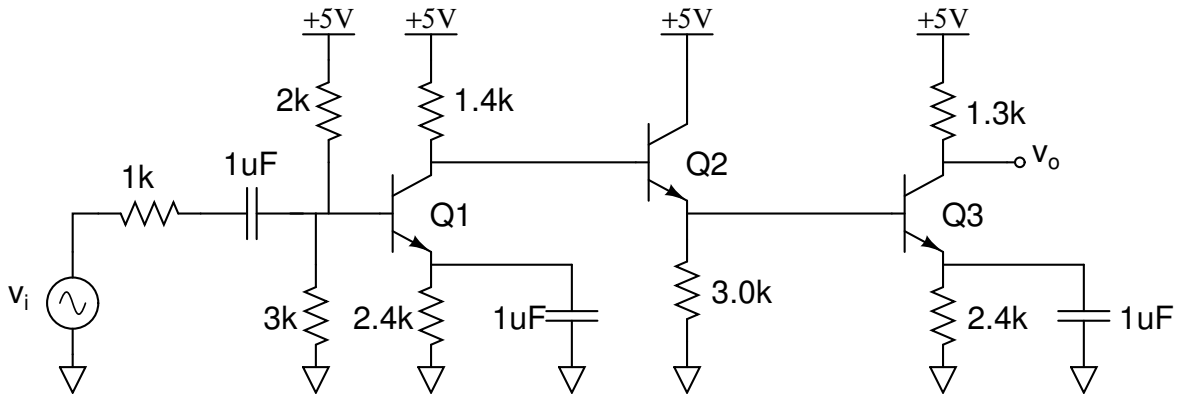
1. Lundberg sections 4 and 5.
2. Grebene section 5.1.
3. Gray and Meyer section 3.5.

Problem 1: Find the mid-band gain for each circuit below. Assume that $\beta = 400$, $V_{BE,ON} = 0.6V$, and ignore r_o .

(a) Circuit a

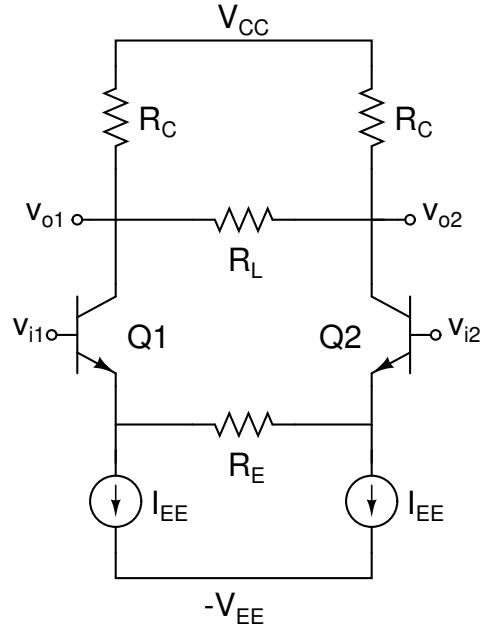


(b) Circuit b



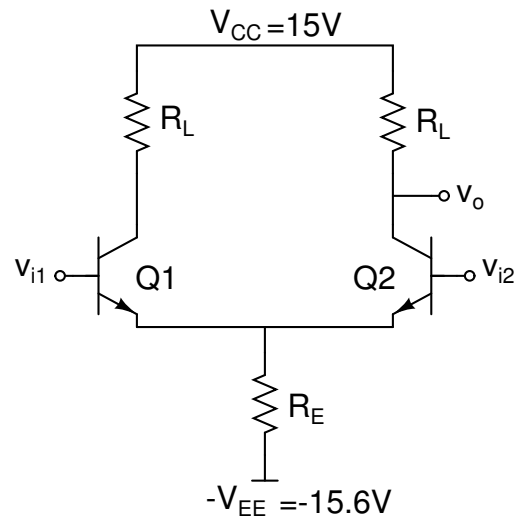
Problem 2: Simulate the CE-EF-CE amplifier in Circuit 1b (above) with HSPICE. Use the following data for your simulations: $I_S = 10^{-15} \text{ A}$, $\beta_F = 200$, $V_A = 100$, $\tau_F = 0.1 \text{ ns}$, $c_{je0} = 10 \text{ pF}$, and $c_{jco} = 2 \text{ pF}$. Turn in your HSPICE input file, and an Awaves plot showing the low and high frequency roll-offs.

Problem 3: For the differential amplifier shown below:



- (a) Find the differential voltage gain a_{vd} and the common mode voltage gain a_{vc} .
- (b) Find both the differential and common mode input and output resistances ($R_{in,d}$, $R_{in,c}$, $R_{out,d}$, and $R_{out,c}$).

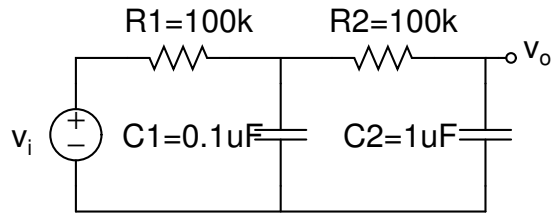
Problem 4: For the single-ended differential amplifier shown below, assume that $\beta = 200$ and $V_{BE,ON} = 0.6V$ for both transistors, and that the DC common mode input voltage is zero. Neglect r_o for this problem.



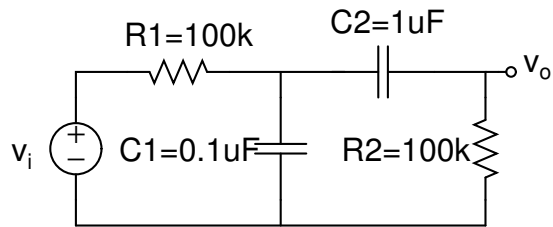
- (a) Express the differential voltage gain a_{vd} as a function of the voltage drop V_L across R_L .
- (b) If $V_{CE,SAT} = 0.3V$, what is the maximum a_{vd} possible?
- (c) Select R_L and R_E so that $R_{in,d} = 1M\Omega$ and $a_{vd} = 300$. What is the common mode rejection ratio (CMRR)?

Problem 5: For each circuit below, find the transfer function v_o/v_i , and draw the Bode plot (magnitude and phase).

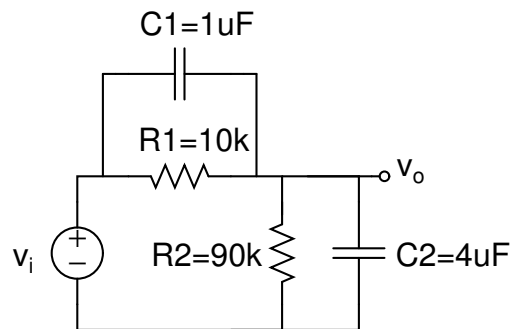
(a) Circuit a



(b) Circuit b



(c) Circuit c



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